

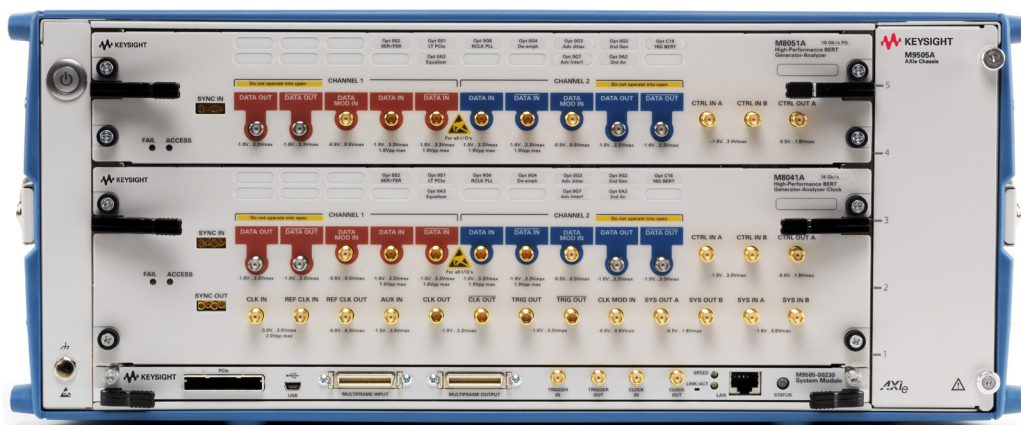
J-BERT M8020A High-Performance BERT

Data Sheet

Version 3.0

NEW

Eye diagram measurements
Bit recovery mode
Add ISI and Jitter with AWG



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Introduction

The high-performance Technologies, Inc. J-BERT M8020A enables fast and accurate receiver characterization of single- and multi-lane devices running up to 16 or 32 Gb/s.

With today's highest level of integration, the M8020A streamlines your test setup. In addition, automated in situ calibration of signal conditions ensures accurate and repeatable measurements. And, through interactive link training, it can behave like your DUT's link partner. All in all, the J-BERT M8020A will accelerate insight into your design.

Key features:

- Data rates up to 8.5 and 16 Gb/s expandable to 32 Gb/s
- 1 to 4 BERT channels in a 5-slot AXIe chassis
- Integrated and calibrated jitter injection: RJ, PJ1, PJ2, SJ, BUJ, sinusoidal level interference (common-mode and differential-mode), SSC (triangular and arbitrary, residual) and Clock/2
- 8 tap de-emphasis, positive and negative
- Integrated and adjustable ISI
- Interactive link training for PCI Express
- Built-in clock recovery and equalization
- All options and modules are upgradeable

Applications:

The J-BERT M8020A is designed for R&D and test engineers who characterize and verify compliance of chips, devices, boards and systems with serial I/O ports up to 16 Gb/s and 32 Gb/s in the consumer, computer, mobile computing, datacenter and communications industry.

The J-BERT M8020A can be used to test popular serial bus standards, such as PCI Express®, SATA/SAS, DisplayPort, USB Super Speed, MIPI® M-PHY®, SD UHS-II, Fibre Channel, QPI, memory buses, backplanes, repeaters, active optical cables, Thunderbolt, 10/40 GbE/SFP+/QSFP, 100GbE/CFP2.

M8000 Series of BER Test Solutions

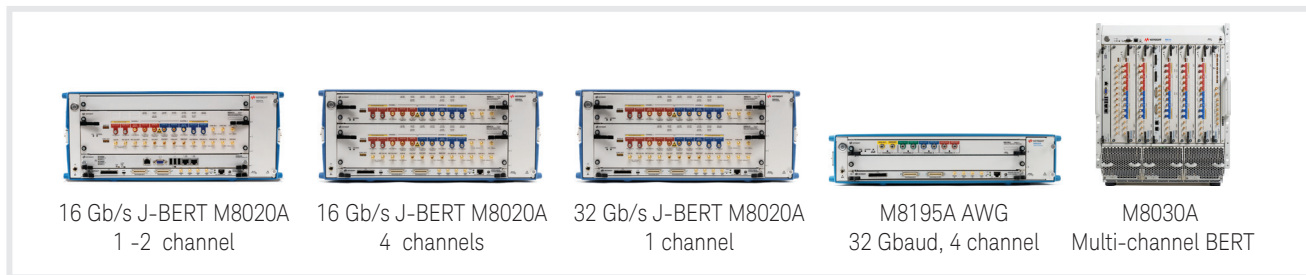
Simplified time-efficient testing is essential when you are developing next-generation computer, consumer, or communication devices.

The M8000 Series is a highly integrated BER test solution for physical layer characterization, validation, and compliance testing.

With support for a wide range of data rates and standards, the M8000 Series provides accurate, reliable results that accelerate your insight into the performance margins of high-speed digital devices.

Shift into high gear with the M8000 Series and take the design verification express lane.

M8000 Series of BER test solutions Highly integrated and scalable for simplified, time efficient testing



- Multi-channel applications
- Interactive link training
- Analyzer equalization and clock recovery
- In situ calibration, de-embedding
- Expandable to higher data rates up to 32 Gb/s
- Higher integration: 16G BERT with 1-4 channels, jitter, de-emphasis



Figure 1. The M8000 Series BER Test Solution is highly integrated and scalable to address the test challenges of the next generation of high-speed digital receiver test.

J-BERT M8020A high-performance BERT

Enabling fast, accurate receiver characterization of single- and multi-lane devices running up to 16 or 32 Gb/s.

Highest level of integration for streamlined test setups

With J-BERT M8020A all receiver (RX) test capabilities are built-in: jitter sources, "common- and differential-mode level interference, and de-emphasis to emulate the transmitter (TX) of the device under test (DUT). In addition M8020A provides a built-in reference clock multiplier for synchronization of the BERT pattern generator with the DUT's reference clock which can carry spread spectrum clocking (SSC). On the analyzer side an equalizer to open closed eyes and a clock recovery with adjustable loop bandwidth for the analyzer is built-in.

With this high level of integration a receiver test set-up with M8020A is now much easier to connect and more robust. Set up and debug time is shortened, calibration is simpler and the frequency of recalibration is lower, resulting in more efficient use of overall test time.

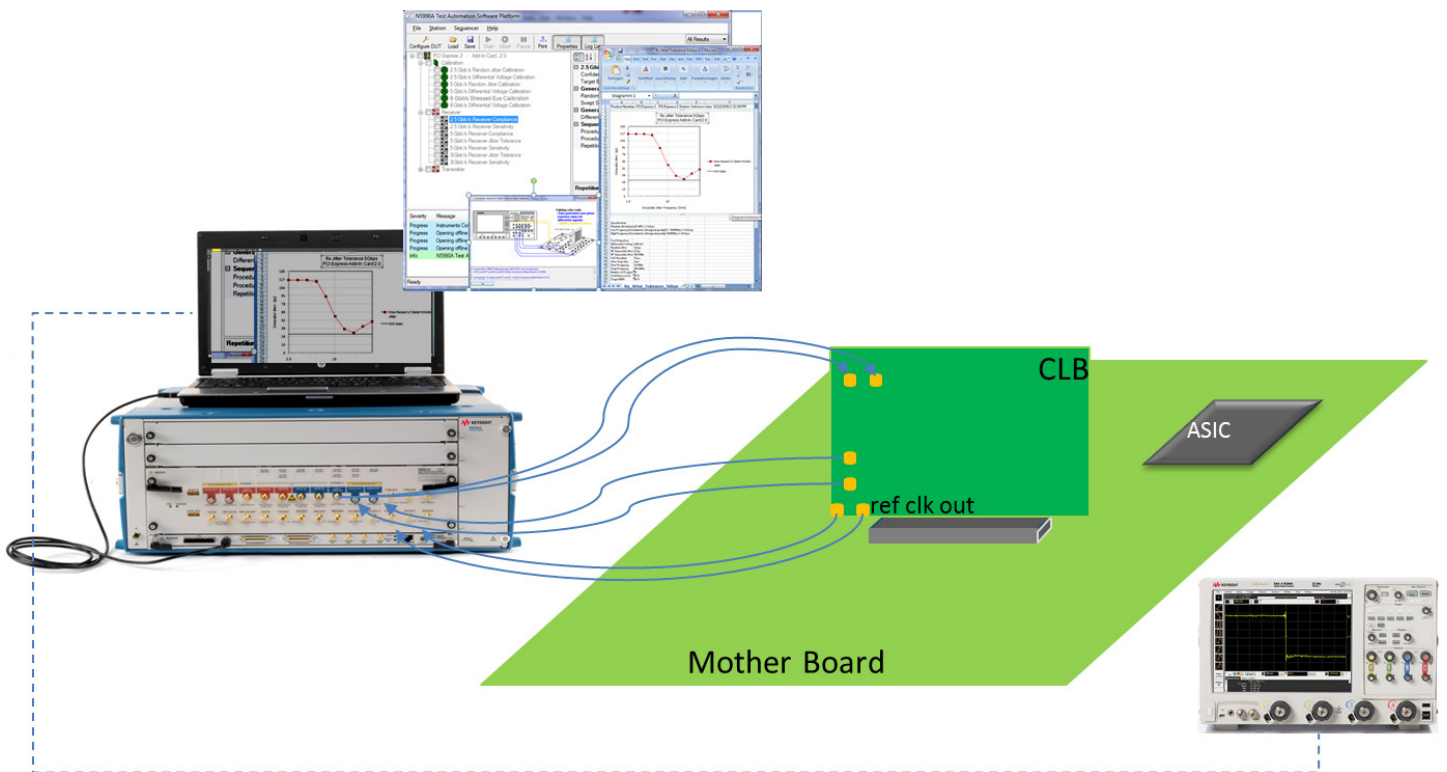


Figure 2. J-BERT M8020A streamlines complex receiver test setups. The example shows a PCIe 3 (8 GT/s) mother board RX test (CEM spec) with J-BERT M8020A connected via a compliance load board (CLB). J-BERT M8020A provides built-in de-emphasis, jitter sources, common-mode and differential mode interference (CMI, DMI), reference clock multiplier, clock recovery and continuous time linear equalizer (CTLE) – everything that is needed is built-in and calibrated.

In situ calibration for the most accurate and repeatable results

At data rates above 5 Gb/s, the influence of the channel (PC-board, cable, connectors) between transmitter (TX) and receiver (RX) is no longer negligible. The reference point for the RX specification moves to the RX input, the test set-up typically has to contain a certain channel characteristic, often an ISI channel, as well. To accurately inject a defined stress condition to the RX in situ calibration is required: at that same exact point where the receiver under test has to be connected during test, a reference load is connected instead and the generated signal is measured. This allows calibration of the test signal at that point where the specification applies by adjusting the instrument generated stress such as jitter in a way that the target signal with all its ingredients is achieved.

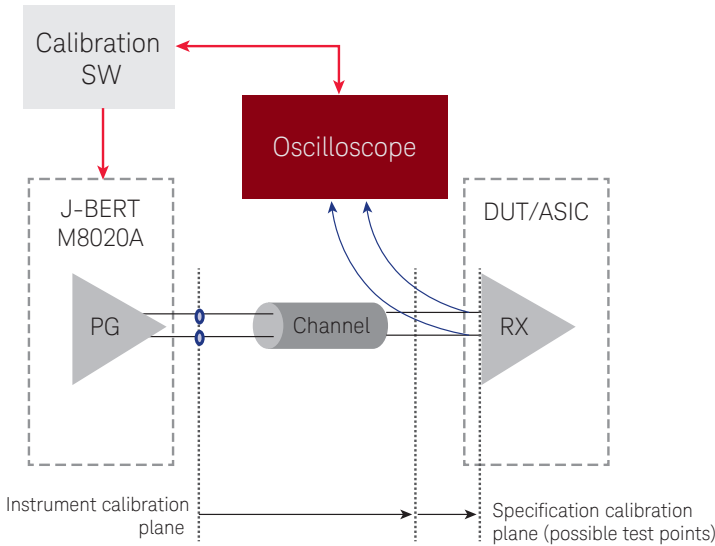


Figure 3. With increasing bit rates the calibration plane for the receiver stress conditions moves closer to the receiver inputs. J-BERT M8020A supports in situ calibration to achieve higher accuracy of the signal and stress conditions at the relevant definable test point.

Interactive link training to fasten loopback

The ever increasing data rate of computer buses and datacom interfaces results in shrinking margins and the necessity to use equalization techniques in transmitters and receivers to compensate for the lossy channels caused by inexpensive PC board material or long cables. For the latest industry standards, such as PCI Express 3 or 4, SAS 12G, and backplanes such as 100GBASE-KR4, the link partners are required to optimize the TX de-emphasis and RX equalization combination. The RX takes the active part during this procedure. In order to do so, the BERT must be capable to understand the low level protocol and to react accordingly, i.e. change its TX de-emphasis as requested. J-BERT M8020A can behave like a real link partner with its interactive link training capability, initially PCIe is supported.

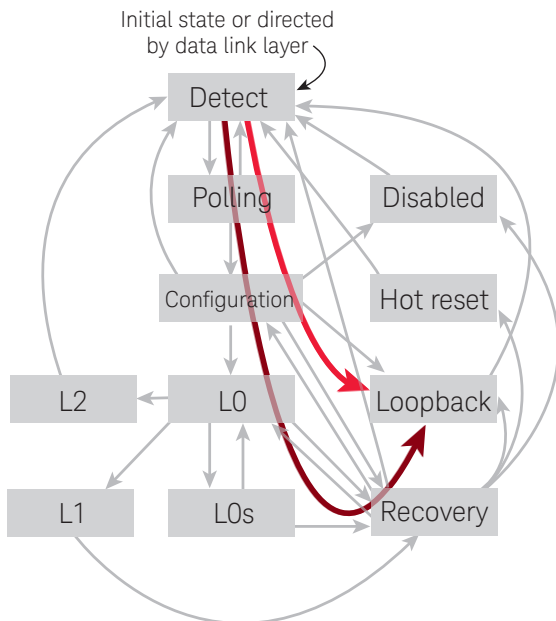


Figure 4. J-BERT M8020A can behave like a real link partner. Due to its interactive link training capability it is able to train the device into the loopback state via recovery state, as shown in this example for PCIe.

Overview J-BERT M8020A High-performance BERT

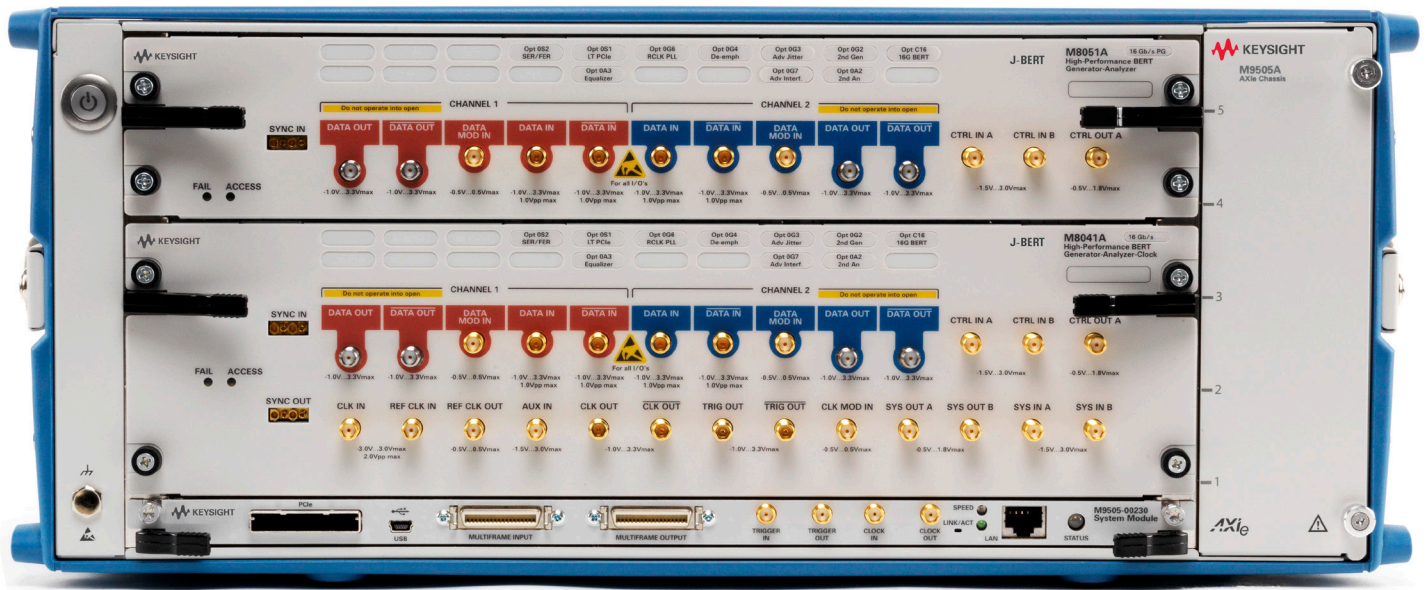


Figure 5. J-BERT M8020A high-performance BERT for accelerated receiver characterization. The configuration shows a 4 channel 16 Gb/s BERT in a 5-slot AXIe chassis consisting of one M8041A module with two BERT channels and clock synthesizer and one M8051A extender module with two additional BERT channels.

Receiver characterization and compliance test

Most multi-gigabit digital interfaces define a receiver tolerance test where the receiver must detect the incoming data bits properly while a certain amount of stress is applied. J-BERT M8020A provides calibrated and built-in jitter sources and automated jitter tolerance measurements. Users can define the modulation frequency range, the number of frequency steps, the min. and max. applied jitter, BER and confidence level and relax time. Results can be exported.

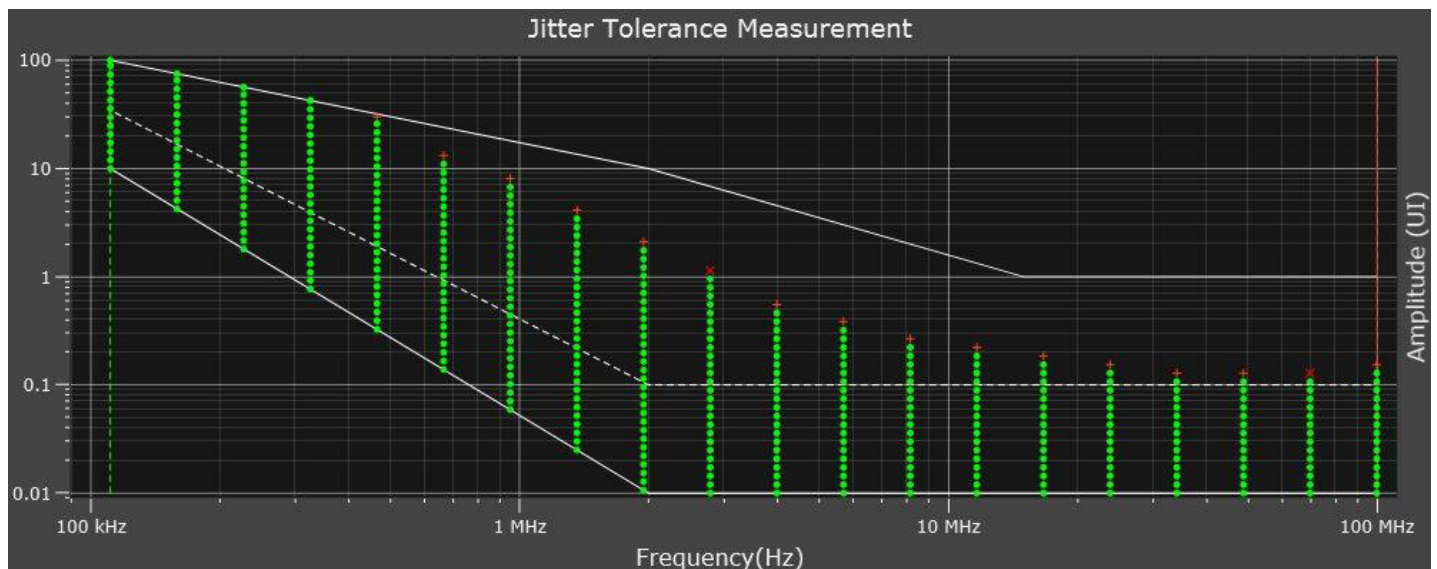


Figure 6. J-BERT M8020A provides automated jitter tolerance characterization and compliance measurements. A library of Jitter tolerance templates is available. To optimize test time, customized jitter tolerance templates can be created with a graphical jitter tolerance template editor. The red dots in the result screen show where the BER level was exceeded, the green dots show where the DUT tolerated the received jitter.

Emulate de-emphasis and compensate for channel loss

Most serial interfaces that operate above 5 Gb/s use transmitters with de-emphasis to compensate for electrical signal degradations caused by printed circuit boards or cables between the transmitter and the receiver ports. R&D and test engineers who need to characterize receiver ports under realistic and worst case conditions require a pattern generator that allows to accurately emulate transmitter de-emphasis and the channel with adjustable 8-tap de-emphasis levels.

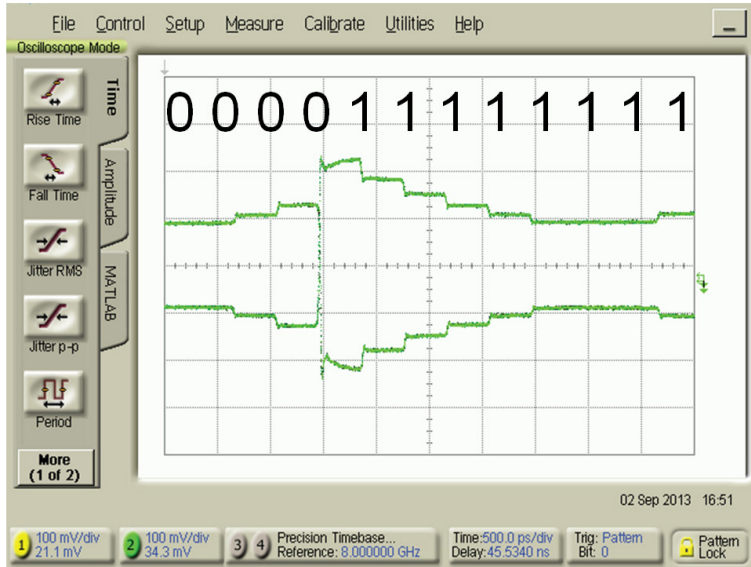


Figure 7. J-BERT M8020A provides built-in de-emphasis with up to 8 taps to emulate a transmitter de-emphasis and to compensate for channel loss. The example shows a bit sequence of eight "0"s and eight "1"s with two pre-cursors and 5 post-cursors that can be adjusted individually.

Emulate channel loss with integrated and adjustable ISI

With increasing data rates the channel loss between transmitter and receiver in digital designs becomes more and more important. The loss is caused by printed circuit board traces, connectors and cables in the signal path. This channel loss results in intersymbol interference (ISI) that depends on the channel material and dimensions, the data rate and the bit pattern. All high-speed digital receivers are specified to tolerate a certain amount of loss or ISI. J-BERT M8020A provides integrated and adjustable ISI to emulate channel loss on all channels during receiver characterization.



Figure 8. J-BERT M8020A offers integrated and adjustable ISI to emulate channel loss. ISI can be controlled for each channel independently via a graphical user interface. Frequency and loss points can be set. S-parameter files can be imported. The example shows a loss curve in blue for the imported S21 parameters for the 12.8 " trace of M8048A. The red line shows the loss parameter entry for M8020A.

J-BERT M8020A configuration for 32 Gb/s

The J-BERT M8020A can be configured as a full 32 Gb/s BERT for accurate receiver characterization. It provides built-in jitter sources, up to 8-tap de-emphasis, and a clock recovery for full-sampling BER and jitter tolerance measurements up to 32 Gb/s. One common user interface allows controlling all parameters of the 32 Gb/s pattern generator and analyzer.

Key features of the 32 Gb/s BERT configuration:

- Excellent intrinsic jitter performance
- Calibrated jitter sources up to 1 UI eye closure for HF jitter, multi-UI LF jitter, BUJ and Clk/2 jitter
- No step increase when turning on jitter sources
- Built-in adjustable ISI (only with M8062A)
- 8 tap de-emphasis with positive and negative cursors
- Superposition of level interference avoids external adders
- Clock recovery with adjustable loop bandwidth (built-in only with M8062A, N4877A is needed for setups with M8061A mux)
- Built-in Analyzer CTLE (only with M8062A)
- Add-on to 16 Gb/s BERT configuration
- Common user interface

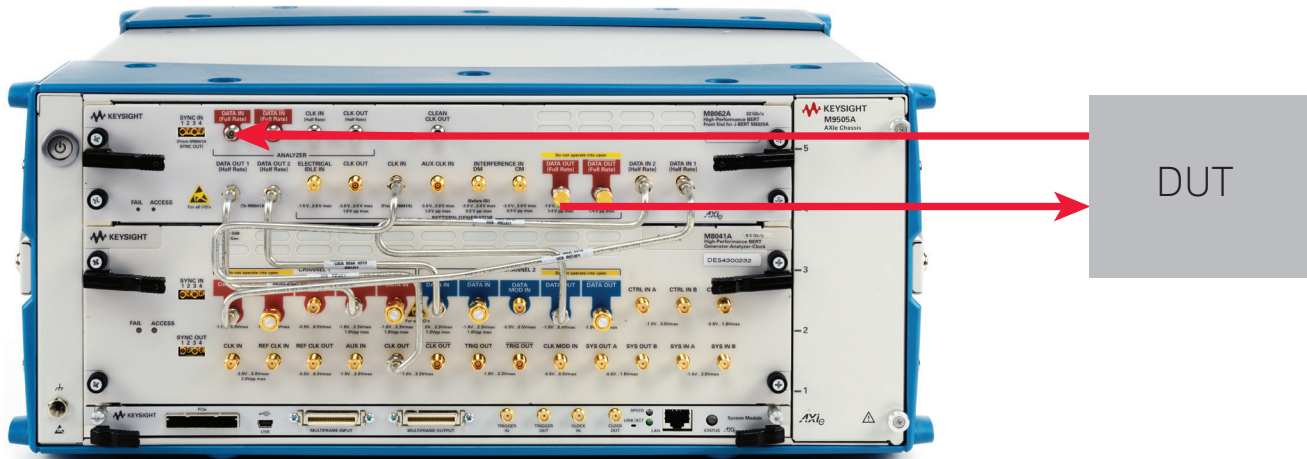


Figure 9. The J-BERT M8020A can be configured as a complete 32 Gb/s BERT for accurate receiver characterization. The M8062A 32Gb/s front-end provides a pattern generator with de-emphasis and ISI injection and analyzer CDR and CTLE.

User interface and measurements

The screenshot displays the J-BERT M8020A software interface. The main window is titled 'M8070A' and features a menu bar (File, Application, System, Clock, Generator, Analyzer, Patterns, Measurements, Utilities, Window, Help) and a toolbar. The central area shows a block diagram of the system, including components like Data Generation, HF Jitter, LF Jitter, Sweep, ISI, Interference 1, PLL Synthesizer, and CDR. The right-hand side contains a 'Parameters' panel for 'Jitter Sweep' and 'Intersymbol Interference .DataOut1', with settings for State (On), Preset (Custom), Mode (One Point), Frequency (8.000 GHz), Insertion Loss (-14.5 dB), and Slope (-1.81 dB/GHz). Below the diagram is a 'Status Indicators' section with a table and control buttons.

| Module | Channel | Bit Rate | Generator | | | Analyzer | | | | | |
|--------|---------|-------------|-----------|--------|--------|----------|------------|-----------|------------|-----------|--------------|
| | | | Data | Output | Jitter | Data | CDR Unlock | Data Loss | Symbol Los | Sync Loss | Error Ratio |
| M1 | 1 | 16.000 Gb/s | Block 1 | ● | ● | Block 1 | ● | ● | ● | ● | BER 0.00e+00 |
| | 2 | 16.000 Gb/s | Block 1 | ● | ● | Block 1 | ● | ● | ● | ● | BER 0.00e+00 |

Control buttons at the bottom include Output, Jitter, SSC, Stopped, and Clk Loss.

Figure 10. The graphical user interface for J-BERT M8020A offers multiple views that can be defined by the user. This example shows the system view on left side and the pattern generator data output parameters at the right.

The multi-channel BERT offers pattern generation and analysis of up to 10 channels in parallel. All impairments can be added to the data signal on each channel individually.

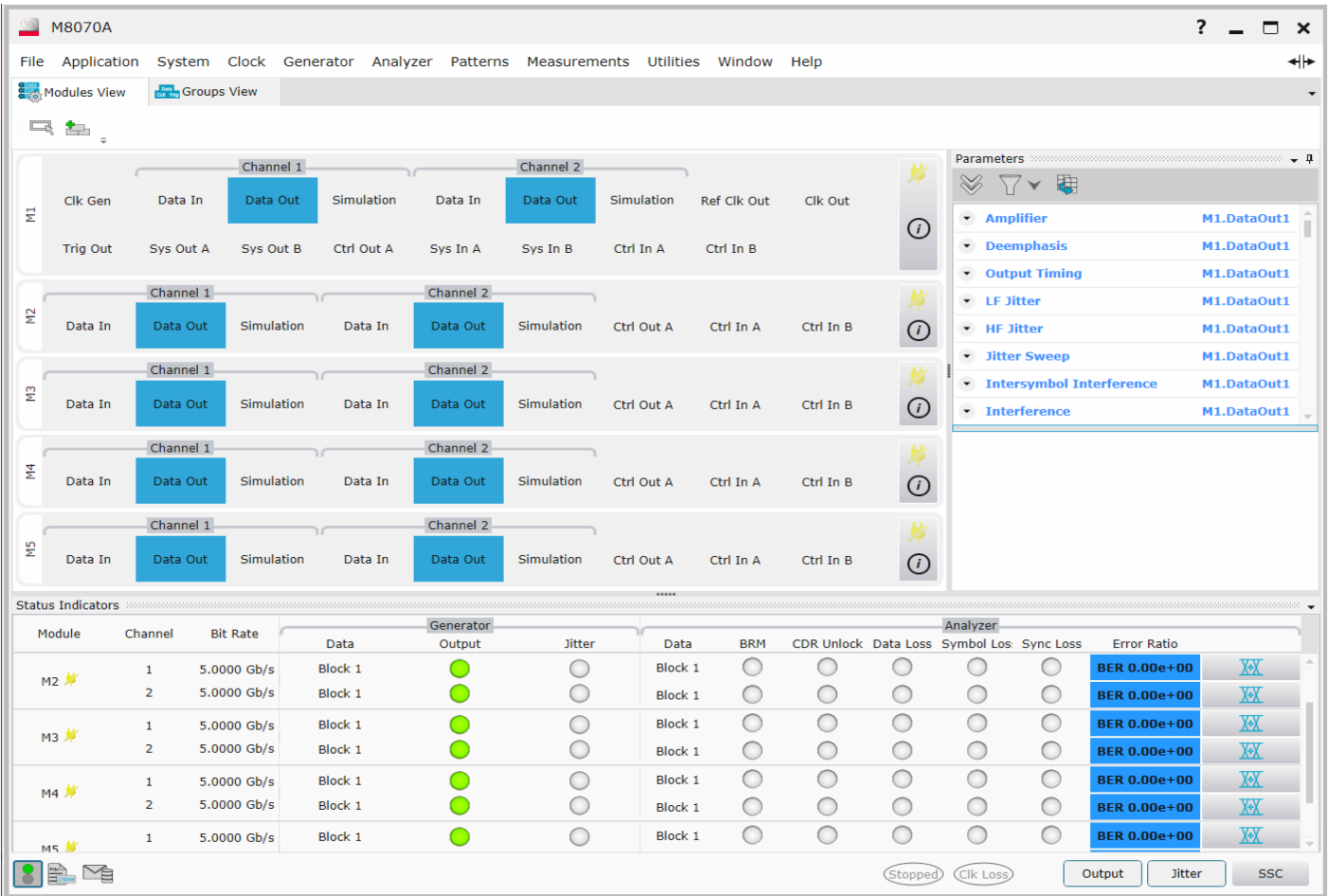


Figure 11. Multiple M8030A 10 channel module view

Eye diagram measurements are important to get a fast overview on the signal quality of the signal at the input of the Analyzer. This can be either the direct output of a transmitter or a distorted signal at the end of a cable or trace. Many signal parameters like rise/fall times, eye height and eye width, as just a few examples, are provided with this measurement tool.

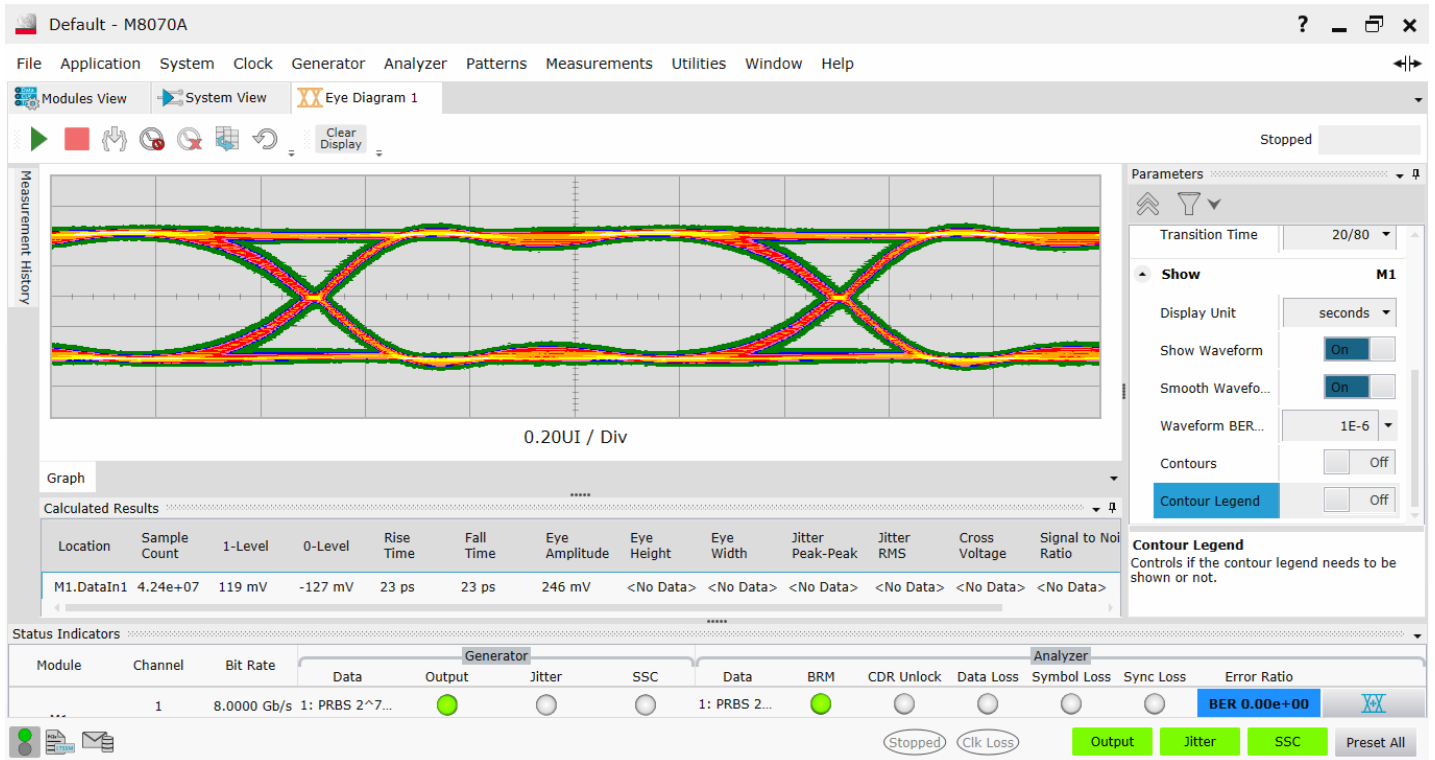


Figure 12. Eye diagram measurement with J-BERT M8020A Analyzer

Pattern sequencer, coding and interactive link training

To simplify test pattern creation, J-BERT M8020A provides unique tools such as an interactive link training state machine, pattern sequencer with break and branch conditions, a real-time scrambler for coded patterns, masking, symbol filtering for meaningful BER measurements for retimed loop back, a library of pre-defined patterns and loop-back sequences, and a graphical pattern editor.

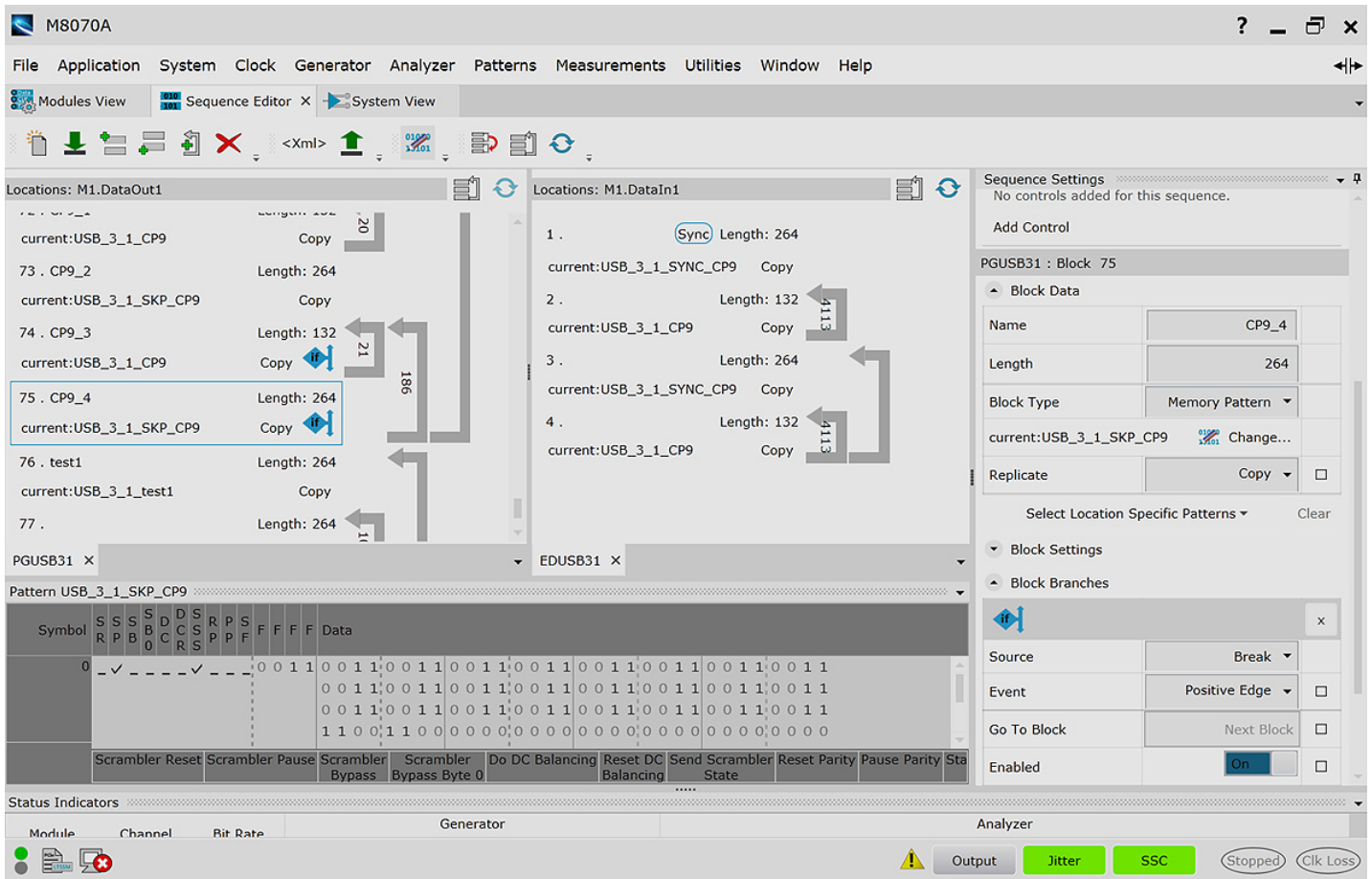


Figure 13. The J-BERT M8020A provides powerful pattern sequencing capabilities. For each pattern generator and analyzer channel a pattern sequence with multiple loop levels, breaks and block controls can be defined. A library of link training sequences for popular standards is available. The example shows a USB 3.1 link training sequence.

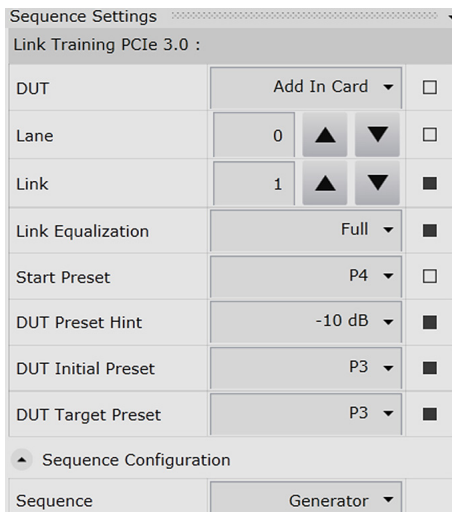


Figure 14. The interactive link training capability of J-BERT M8020A significantly reduces the effort to generate and tune a loopback sequence for your device under test. The example shows the properties you can choose for the PCIe3 link training state machine.

Accuracy and performance

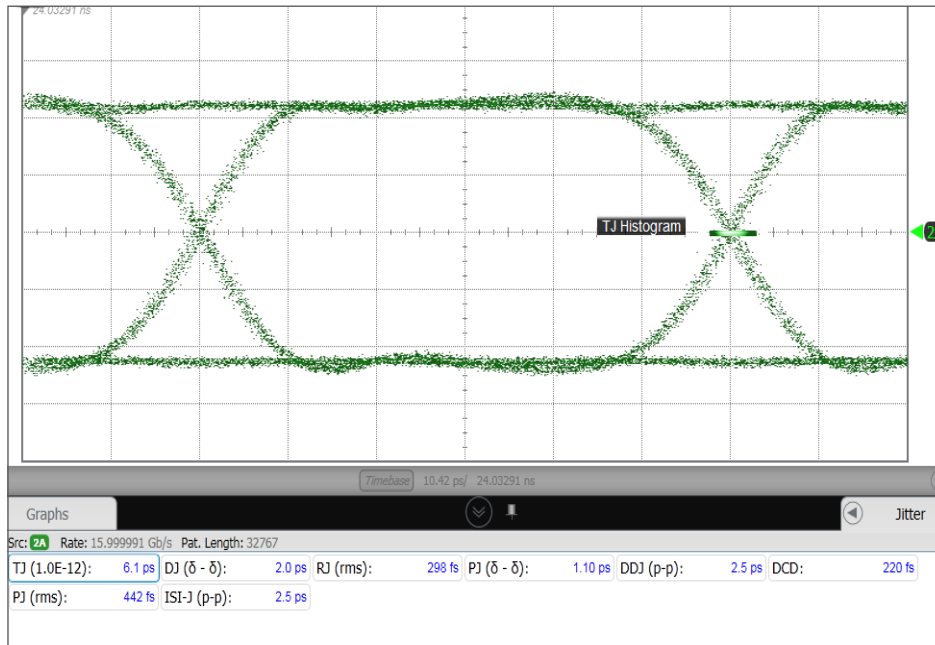


Figure 15. Clean 16.0 Gb/s output signal of J-BERT M8020A with M8041A BERT module using its internal clock source and PRBS $2^{15}-1$ pattern.

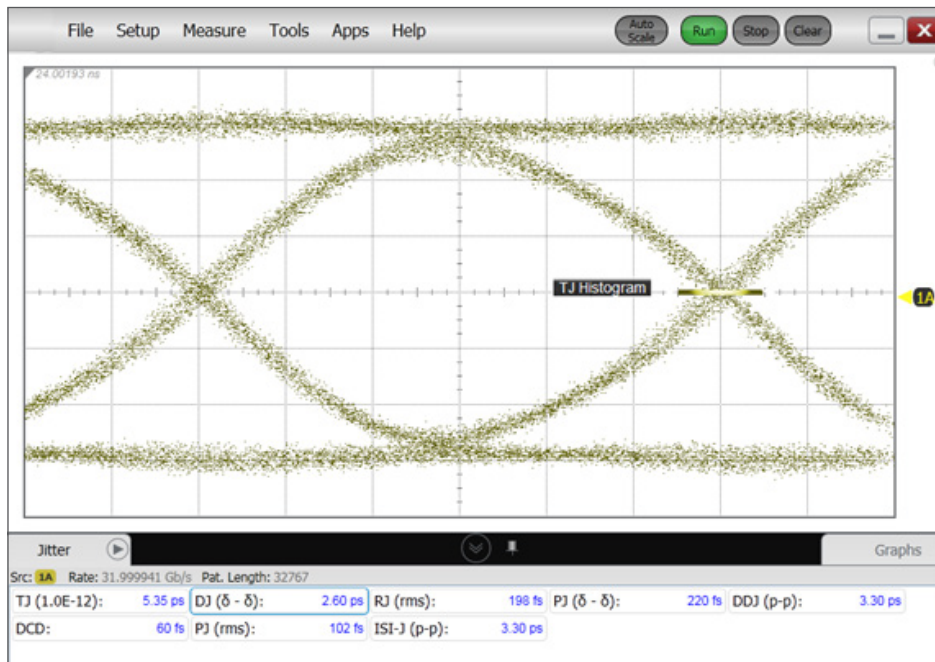


Figure 16. The 32 Gb/s output signal shows excellent intrinsic jitter. This shows the output signal of M8061A when used with M8041A BERT module and its internal clock source and PRBS $2^{15}-1$ pattern, and the band pass filter M8061A-803 in the clock path.

Specifications for M8041A and M8051A J-BERT high-performance BERT modules

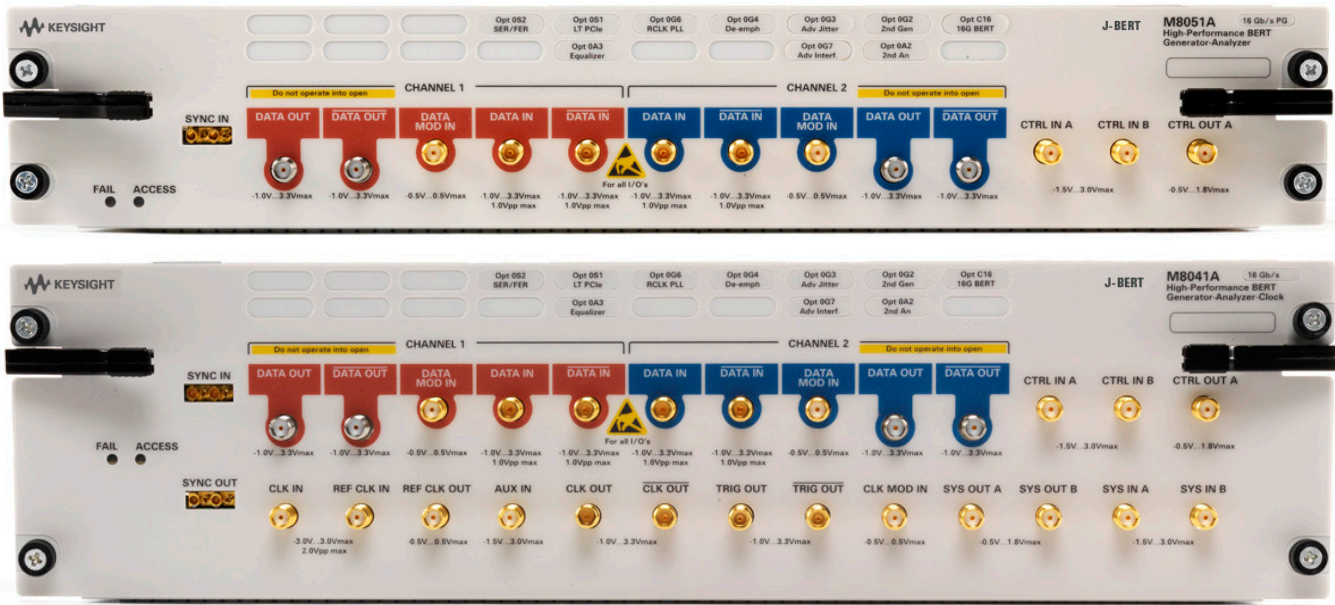
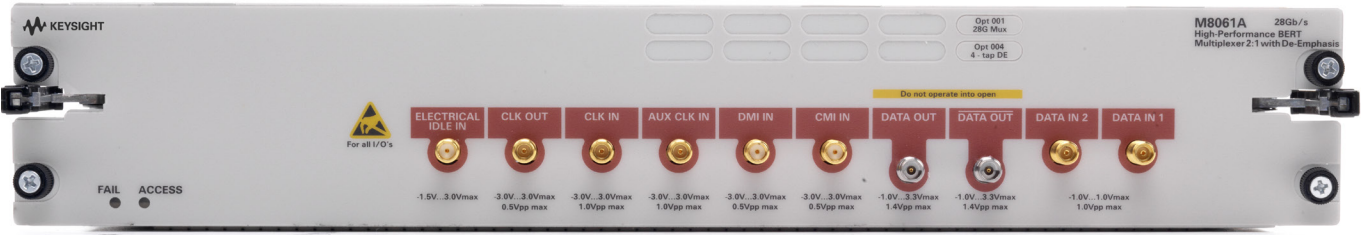


Figure 17. Front panel view of M8041A module (bottom) and M8051A (top).

Specifications for M8061A 32Gb/s multiplexer with de-emphasis

Please refer to M8061A data sheet (5991-2506EN) for specification details.



Specifications for M8062A 32Gb/s BERT Front-end

Please refer to M8062A data sheet (5992-0987EN) for specification details.



Specifications pattern generator

Data output (DATA OUT 1, DATA OUT 2)

Table 1. Data output characteristics for M8041A and M8051A.

| All timing parameters are measured @ 0.5 V into ground | | M8041A | M8051A |
|---|---|---------------|---------------|
| Data rate | 256 Mb/s to 8.50 Gb/s (opt. G08 or C08), 256 Mb/s to 16.20 Gb/s (opt. G16 or C16) | X | X |
| Data format | NRZ | | |
| Channels per module | 1 or 2 (second channel requires opt. OG2) | | |
| Amplitude | 50 mV to 1.2 V _{pp} single ended, 100 mV to 2.4 V _{pp} differential, 1 mV resolution; addresses LVDS, CML, low-voltage CMOS, others. See table 2 for max. output amplitude in presence of CMI or DMI | | |
| Amplitude accuracy | 5% ± 5 mV typical (AC) ³ | | |
| Output voltage window | -1 V to +3.0 V | | |
| External termination voltage | -1 V to +3.0 V. For offset > 1.3 V the termination voltage should be ± 0.5 V of offset | | |
| Transition time | Steep: 12 ps typical (20%-80%) ⁶ Moderate: 17 ps typical (20%-80%) Smooth: 20 ps typical (20%-80%) | | |
| Crossing point | Adjustable from 30% to 70% | | |
| Intrinsic total jitter ¹ | 8 ps p-p typical | | |
| Intrinsic random jitter ² | 300 fs rms typical | | |
| Data delay range | 0 to 10 ns, resolution 100 fs | | |
| Data delay accuracy | ±1% ±20 mUI typical ⁵ | | |
| Deskew accuracy | ±10 ps typical between data out 1 and 2 of the same module | | |
| Electrical idle transition time | Output transitions from full swing signal to 0 V amplitude and vice versa at constant offset within 4 ns typical. Electrical idle can be controlled from sequencer. Latency depends on selected coding (symbol width): Binary (1 bit) ±64 UI ± jitter amplitude /2 8B/10B (10 bit) ±80 UI ± jitter amplitude /2 128B/130B (130 bit) ±130 UI ± jitter amplitude /2 128B/132B (132 bit) ±132 UI ± jitter amplitude /2 | | |
| Skew between normal and complement output | 3 ps maximum at front panel, 8 ps maximum at the end of the recommended cable pair (M8041A-801) | | |
| Termination | 50 Ω into GND or external termination voltage. Do not operate into open. Unused outputs must be terminated into termination voltage. | | |
| Output protection | This is an emergency shut down feature. It disables an output in case an unexpected voltage is detected. DC coupling mode: Termination range for devices connected to data out: – unbalanced 50 Ω ± 10 Ω typical – balanced 100 Ω ± 20 Ω typical Operation into open is possible for these ranges when “DC coupled“ and “balanced“ termination modes are selected: – output amplitude max. 300 mV ⁴ – offset 0 to 370 mV AC coupling mode: An external DC blocking capacitor is expected. If a resistive load is discovered the output will not be enabled. | | |
| Termination modes | Balanced/unbalanced DC/AC coupling | | |
| Connectors | 3.5 mm, female | | |

1. At 16.2 Gb/s PRBS 2¹⁵-1, BER 10⁻¹², with internal clock.

2. At 16 Gb/s and clock pattern.

3. At 256 Mb/s measured with DCA-X 86108B and clock pattern and in the middle of the eye.

4. Per output when differentially terminated into 100 Ω. Results in doubled swing when driving into open.

5. At constant temperature.

6. Measured with DCA-X 86118A. For serial numbers below DE55300500 for M8041A or M8051A: 15 to 20 ps typical (20%-80%)

Specifications pattern generator (continued)

Data output (DATA OUT 1, DATA OUT 2) (continued)

Table 2. Data output amplitude maximum (single ended) in presence of DMI, CMI, offset voltage.

| Offset ≤ 1.9 V | Offset > 1.9 V | CMI | DMI |
|----------------|----------------|----------|----------------------|
| 1.2 Vpp | 0.9 Vpp | disabled | disabled |
| 0.9 Vpp | 0.675 Vpp | disabled | enabled |
| 0.9 Vpp | 0.75 Vpp | enabled | disabled |
| 0.675 Vpp | 0.562 Vpp | enabled | enabled |
| 0.8 Vpp | 0.666 Vpp | enabled | enabled ¹ |

1. For DMI < 12.5 % of amplitude.

De-emphasis (DATA OUT)

M8020A provides built-in de-emphasis with positive and negative cursors based on a finite impulse response (FIR) filter.

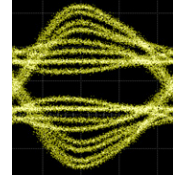
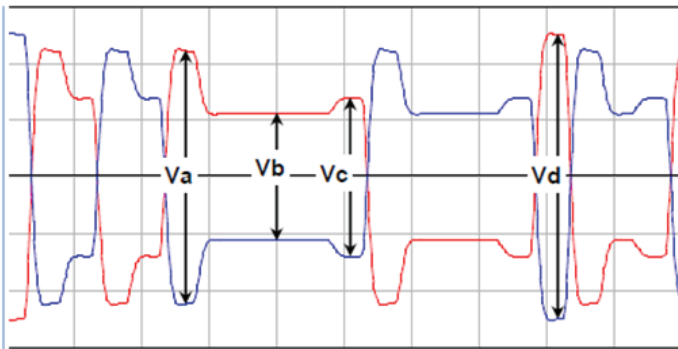


Table 3. Specifications for multi-tap de-emphasis (requires option 0G4).

| | | M8041A | M8051A |
|----------------------------|---|----------|----------|
| De-emphasis taps | 8 (requires opt. 0G4) can be adjusted for each channel independently | | |
| Pre-cursor 2 | ± 6.0 dB | | |
| Pre-cursor 1 | ± 12.0 dB | | |
| Post-cursor 1 | ± 20.0 dB | Opt. 0G4 | Opt. 0G4 |
| Post-cursor 2 | ± 12.0 dB | | |
| Post-cursor 3 | ± 12.0 dB | | |
| Post-cursor 4 | ± 6.0 dB | | |
| Post-cursor 5 | ± 6.0 dB | | |
| De-emphasis tap resolution | ± 0.1 dB | | |
| De-emphasis tap accuracy | ± 1.0 dB ¹ typical | | |

1. Sum of all cursors may not exceed Vpp max. The tap accuracy applies for PCIe 3 presets for pre-cursor 1 and post-cursor 1 at 8 Gb/s.



$$\begin{aligned} \text{Post-cursor 1} &= 20\log_{10} Vb/Va \\ \text{Pre-cursor} &= 20\log_{10} Vc/Vb \\ Vpp \text{ nominal} &= 20\log_{10} Vd \end{aligned}$$

Figure 18. Definition of nominal output amplitude and de-emphasis.

Specifications pattern generator (continued)

Clock output (CLK OUT)

Table 4. Clock output specifications

| | | M8041A | M8051A |
|------------------------------|--|--------|--------|
| Frequency range | 256 MHz to 8.50 GHz (opt. G08 or C08), 256 MHz to 16.20 GHz (opt. G16 or C16) | x | No clk |
| Frequency resolution | 1 Hz | | |
| Frequency accuracy | ± 15 ppm | | |
| Amplitude | 0.1 to 1 V, 5 mV steps, single ended | | |
| Output voltage window | -1 V to +3 V ¹ | | |
| External termination voltage | -1 V to +3.0 V | | |
| Transition times | 20 ps typical (20%-80%) | | |
| Duty cycle | 50%, accuracy ± 15% | | |
| Clock divider | 1, 2, 4, 8, 10, 16, 20, 24, 30, 32, 40, 50, 64, 66, 80. For other dividers use TRG output | | |
| Clock modes | See table 5 | | |
| Intrinsic random jitter | 300 fs rms typical at 16.2 GHz and clock divider = 1 | | |
| SSB phase noise ² | - 85 dBc/ Hz typical at 10 kHz offset and internal clock and 10/100MHz as external reference clock. - 80 dBc/Hz with 10 kHz offset for reference clock multiplier bandwidth 0.1/2/5 MHz | | |
| Termination | 50 Ω into GND or external termination voltage. Do not operate into open. Unused outputs must be terminated into termination voltage. | | |
| Connectors | 3.5 mm, female | | |

- If V_{term} is other than 0 V the following applies:
High level voltage range = $2/3 * V_{\text{term}} - 0.95 \text{ V} < \text{HIL} < V_{\text{term}} + 2 \text{ V}$
Low level voltage range = $2/3 * V_{\text{term}} - 1 \text{ V} < \text{LOL} < V_{\text{term}} + 1.95 \text{ V}$
- For 8.1 to 16.2 GHz clocks.

Table 5. Clock modes (M8041A only).

| Clock mode | Clock generation | Input frequency range | | |
|---|---|-----------------------|---------------------|----------|
| | | Option G08/ C08 | Option G16/ C16 | Option |
| Reference | PLL with bandwidth below 1 kHz | 10/100 MHz | 10/100 MHz | |
| Direct | No PLL | 8.1 GHz to 8.5 GHz | 8.1 GHz to 16.2 GHz | |
| Reference clock multiplier bandwidth 100 kHz | m/n PLL with loop bandwidth 100 kHz m, n = 1 to 1620 | 10 MHz to 8.5 GHz | 10 MHz to 16.2 GHz | |
| Reference clock multiplying PLL with loop bandwidth 2 MHz | Integer PLL with loop bandwidth 2 MHz ¹ | 10 to 105 MHz | 10 to 105 MHz | Opt. 0G6 |
| Reference clock multiplying PLL with loop bandwidth 5 MHz | Integer PLL with loop bandwidth 5 MHz ¹ | 50 to 105 MHz | 50 to 105 MHz | Opt. 0G6 |

- Intended use with settings in Table 7 (other settings may be possible, contact factory)

Specifications pattern generator (continued)

Reference clock input (REF CLK IN)

This input on the M8041A module allows locking the system clock to an external reference clock of 10 or 100 MHz instead of the internal oscillator. It also allows to use an external clock, see clock modes.

Table 6. Reference clock input specifications (M8041A only).

| | | M8041A | M8051A |
|-----------------|--|--------|--------|
| Input amplitude | 0.2 to 1.4 V _{pp} | x | No |
| Input frequency | 10 MHz to 16.2 GHz, depends on clock mode and max. data rate option ¹ | | |
| Interface | Single ended. 50 Ω nominal | | |
| Connector | SMA, female | | |

Table 7. Predefined settings for reference clock multiplier (M8041A with option 0G6 only).

| Ref clock input | Standard | Target data rate | Multiplier | PLL loop BW | M8041A |
|-------------------|-----------------|---|-------------------------------|-------------|----------|
| 100 MHz | PCIe 4 | 16 Gb/s | 160 | 2 MHz | |
| 100 MHz | PCIe 3 | 8 Gb/s | 80 | 5 MHz | |
| 100 MHz | PCIe 2 | 5 Gb/s | 50 | 5 MHz | |
| 100 MHz | PCIe 1 | 2.5 Gb/s | 25 | 5 MHz | |
| 26 MHz to 52 MHz | SD UHS-II | 390 Mb/s to 780 Mb/s | 15 | 2 MHz | |
| 26 MHz to 52 MHz | SD UHS-II | 780 MHz to 1.56 Gb/s | 30 | 2 MHz | |
| 52 MHz to 104 MHz | SD UHS-II Gen 2 | 1.56 Gb/s to 3.12 Gb/s | 30 | 2 MHz | |
| 52 MHz to 104 MHz | SD UHS-II Gen 2 | 3.12 Gb/s to 6.24 Gb/s | 60 | 2 MHz | |
| 19.2 MHz | MIPI M-PHY | 1.248/ 1.4592/ 2.496/ 2.9184/ 4.992/ 5.8368 Gb/s | 65/ 76/ 130/ 152/ 260/ 304 | 2 MHz | Opt. 0G6 |
| 26 MHz | MIPI M-PHY | 1.248/ 1.456/ 2.496/ 2.912/ 4.992/ 5.824 Gb/s | 48/ 56/ 96/ 112/ 192/ 224 | 2 MHz | |
| 38.4 MHz | MIPI M-PHY | 1.248/ 1.4592/ 2.496/ 2.9184/ 4.992/ 5.8368 Gb/s | 65:2/ 38/ 65/ 76/ 130/ 152 | 2 MHz | |
| 52 MHz | MIPI M-PHY | 1.248/ 1.456/ 2.496/ 2.912/ 4.992/ 5.824 Gb/s | 24/ 28/ 48/ 56/ 96/ 112 | 2 MHz | |

1. Note: a minimal slew rate of 0.3 V/ns at the REF CLK IN signal is required to ensure a proper frequency measurement. If this requirement can't be met the input frequency should be set manually.

Supplementary inputs and outputs of M8041A and M8051A

Trigger output (TRG OUT)

The trigger output can be used in different modes:

1. Divided clock, dividers: 2 to 65535
2. Sequence block trigger with adjustable pulse width and offset
3. PRBS sequence trigger with adjustable pulse width

Table 8. Trigger output specifications (M8041A only).

| | | M8041A | M8051A |
|------------------------------|---|--------|--------|
| Amplitude | 0.1 to 1 V _{pp} single ended; 0.2 to 2 V _{pp} differential | | |
| Output voltage window | -1 to 3 V ¹ | x | No trg |
| External termination voltage | -1 to 3 V | | |
| Interface | Differential, 50 Ω | | |
| Connector | 3.5 mm, female | | |

1. If V_{term} is other than 0 V the following applies:

$$\text{High level voltage range} = 2/3 * V_{\text{term}} - 0.95 \text{ V} < \text{HIL} < V_{\text{term}} + 2 \text{ V}$$

$$\text{Low level voltage range} = 2/3 * V_{\text{term}} - 1 \text{ V} < \text{LOL} < V_{\text{term}} + 1.95 \text{ V}$$

Reference clock output (REF CLK OUT)

Outputs a 10 and 100 MHz clock, 1 V_{pp} single ended into 50 Ω. M8041A only.

Connector: SMA, female.

Clock input (CLK IN)

For future use. For M8041A only. See reference clock input for direct clock mode.

Control input A and B (CTRL IN A, CTRL IN B)

Functionality of each input can be selected as: sequence trigger, error add and pattern capture event.

Table 9. Control input specifications (M8041A and M8051A).

| | | M8041A | M8051A |
|----------------------|---------------|--------|--------|
| Input voltage | -1 V to +3 V | | |
| Termination voltage | -1 V to +3 V | | |
| Threshold voltage | -1 V to +3 V | x | x |
| Delay to data output | See Figure 15 | | |
| Connector | SMA, female | | |

Control output A (CTRL OUT A)

Outputs a pulse in case of an error. Generates a pulse or static high/low if used from sequencer.

Note: Control output functionality is not available with M8061/2A, only Sync outputs are available

Table 10. Control output specifications (M8041A and M8051A).

| | | M8041A | M8051A |
|-----------------------------|---|--------|--------|
| Amplitude ¹ | 0.1 to 2 V | | |
| Output voltage ¹ | -0.5 to 1.75 V | | |
| Delay to data output | CTRL Out to DATA Out alignment depends on the selected coding (symbol width): | | |
| | Binary (1 bit) ±64 UI ± jitter amplitude /2 | x | x |
| | 8B/10B (10 bit) ±80 UI ± jitter amplitude /2 | | |
| | 128B/130B (130 bit) ±130 UI ± jitter amplitude /2 | | |
| | 128B/132B (132 bit) ±132 UI ± jitter amplitude /2 | | |
| Connector | SMA, female | | |

1. When terminated with 50 Ω into GND. Doubles into open.

Supplementary inputs and outputs of M8041A and M8051A (continued)

Synchronization input and output (SYNC IN, SYNC OUT)

The Sync output on M8041A: clock output to synchronize multiple modules to a common clock.

The Sync input is a clock input on M8051A module to synchronize additional modules to a common clock.

A sync cable is delivered with each M8051A module by default.

System input A/B and auxiliary input (AUX IN)

Control inputs to synchronize events for the pattern sequencer.

Auxiliary input: for future use. For M8041A only.

Table 11. System input and auxiliary input specifications (M8041A only)

| | | M8041A | M8051A |
|----------------------|---------------|--------|--------|
| Input voltage | -1 V to +3 V | | |
| Termination voltage | -1 V to +3 V | | |
| Threshold voltage | -1 V to +3 V | x | No |
| Delay to data output | See Figure 15 | | |
| Connector | SMA, female | | |

System output A/B (SYS OUT A/B)

Generates a pulse or static high/low controlled by the pattern sequencer.

Note: Control output functionality is not available with M8061/2A, only Sync outputs are available

Table 12. System output specifications (M8041A only).

| | | M8041A | M8051A |
|-----------------------------|---|--------|--------|
| Amplitude ¹ | 0.1 to 2 V | | |
| Output voltage ¹ | -0.5 to 1.75 V | | |
| Delay to data output | SYS Out to DATA Out alignment depends on the selected coding (symbol width): Binary (1 bit) ±64 UI ± jitter amplitude /2 8B/10B (10 bit) ±80 UI ± jitter amplitude /2 128B/130B (130 bit) ±130 UI ± jitter amplitude /2 128B/132B (132 bit) ±132 UI ± jitter amplitude /2 | x | No |
| Connector | SMA, female | | |

1. When terminated with 50 Ω into GND. Doubles into open.

Delay of SYS IN and CTRL IN to the data outputs in UI = block length [UI] + X ± LFPJ [UI] * 0.5 ± SSC deviation [UI]

The SSC deviation can be calculated as:

down spread SSC deviation = (data rate * (deviation in %/100)) / (8*SSC modulation frequency)

center spread SSC deviation = (data rate * (deviation in %/100)) / (4*SSC modulation frequency)

| X in UI typical | Data rate | Coding (symbol width) | binary (1 bit) | 8B/10B (10 bit) | 128B/130B (130 bit) | 128B/132B (132 bit) |
|-----------------|----------------------------|-----------------------|----------------|-----------------|---------------------|---------------------|
| | | | | | | |
| CTRL IN to DATA | 256 to 506.25 Mb/s | | 4672 | 4800 | 5330 | 5280 |
| | 506.25 Mb/s to 1.0125 Gb/s | | 5568 | 5760 | 6240 | 6204 |
| | 1.0125 to 2.025 Gb/s | | 7680 | 7920 | 8450 | 8382 |
| | 2.025 to 4.05 Gb/s | | 11840 | 12064 | 12740 | 12805 |
| | 4.05 to 8.1 Gb/s | | 20013 | 20336 | 21321 | 21384 |
| | 8.1 to 16.2 Gb/s | | 36544 | 37098 | 38515 | 38664 |
| SYS IN to DATA | 256 to 506.25 Mb/s | | 4992 | 5120 | 5590 | 5676 |
| | 506.25 Mb/s to 1.0125 Gb/s | | 6208 | 6400 | 6903 | 6863 |
| | 1.0125 to 2.025 Gb/s | | 8896 | 9200 | 9880 | 9768 |
| | 2.025 to 4.05 Gb/s | | 14291 | 14584 | 15600 | 15629 |
| | 4.05 to 8.1 Gb/s | | 24896 | 25432 | 27040 | 27166 |
| | 8.1 to 16.2 Gb/s | | 46312 | 47294 | 49884 | 50171 |

Figure 19. This table shows typical values for X in unit intervals (UI) in order to calculate the delay between SYS Input and CTRL input to the data outputs of M8041A and M8051A. The X depends on data rate and the selected coding (symbol width).

Jitter tolerance specifications

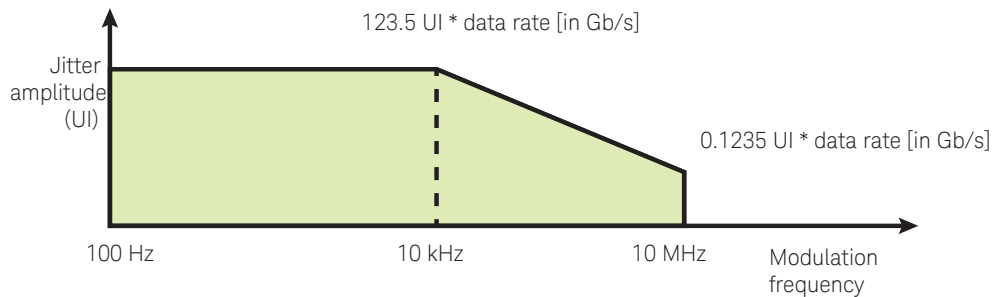
M8020A provides built-in calibrated jitter sources designed to cover receiver test needs for most of the popular multi-gigabit standards such as: PCIe, USB, MIPI, SATA, DisplayPort, CPU frontside buses, CEI, 10GbE, 100GbE, SFP+, QSFP, CFP2/4, etc. M8020A provides automated jitter tolerance measurements. A library of pre-defined compliance curves is provided.

For 32 Gb/s setups using M8061A, the jitter sources of M8041A/51A can be used. The M8061A multiplexer is transparent to jitter. The ranges specified in table 13 to 17 refer to the datarate at the output of M8061A when the mux configuration is selected.

Table 13. Specifications for low frequency periodic jitter (requires option 0G3 advanced jitter sources).

| | | M8041A | M8051A |
|---|---------------------------|---|----------|
| Low frequency periodic jitter (LF PJ) (generated by IQ modulator) | Amplitude range | 0 to 123.5 UI x data rate (in Gb/s) for modulation frequencies of 100 Hz to 10 kHz, see table below. For modulation frequencies between 10 kHz and 10 MHz the maximum LF PJ = $\frac{1.235 \text{ UI} * \text{data rate (Gb/s)}}{\text{modulation frequency (MHz)}}$ | Opt. 0G3 |
| | Frequency | 100 Hz to 10 MHz, Sinusoidal modulation | Opt. 0G3 |
| | Jitter amplitude accuracy | ± 2 % ± 1 ps typical | |
| | Adjustable | For each data channel independently, same LFPJ for clock and trigger | |

Low frequency periodic jitter



| Data rate | Max UI at modulation frequency 100 Hz to 10 kHz | Max UI at modulation frequency 10 MHz |
|----------------------------|---|---------------------------------------|
| 256.0 Mb/s to 506.25 Mb/s | 31.6 to 62.5 UI | 0.0317 to 0.0625 UI |
| 506.25 Mb/s to 1.0125 Gb/s | 62.5 to 125 UI | 0.0625 to 0.125 UI |
| 1.0125 Gb/s to 2.025 Gb/s | 125 to 250 UI | 0.125 to 0.25 UI |
| 2.025 Gb/s to 4.05 Gb/s | 250 to 500 UI | 0.25 to 0.5 UI |
| 4.05 Gb/s to 8.1 Gb/s | 500 to 1000 UI | 0.5 to 1 UI |
| 8.1 Gb/s to 16.2 Gb/s | 1000 to 2000 UI | 1 to 2 UI |

Figure 20. Low frequency periodic jitter maximum depends on data rate and modulation frequency.

Jitter tolerance specifications (continued)

Table 14. Specifications for high frequency periodic jitter, random jitter, spectrally distributed random jitter, bounded uncorrelated jitter, Clock/2 jitter (requires option 0G3 advanced jitter sources).

| | | | M8041A | M8051A |
|---|---------------------------|--|----------|----------|
| High frequency jitter (generated by delay line) | Range | 1 UI p-p for data rates > 1 Gb/s note: this is max sum of RJ, HF-PJ1 and HF-PJ, spectral RJ, external delay modulation and BUJ. | Opt. 0G3 | Opt. 0G3 |
| | Adjustable | For each channel independently | | |
| High frequency periodic jitter (HF PJ1 and HF PJ2) | Range | See HF jitter above ¹ | | |
| | Frequency | 1 kHz to 500 MHz. For data rates < 4 Gb/s the max modulation frequency is data rate / 8. Two tone possible. Sweep. | Opt. 0G3 | Opt. 0G3 |
| | Jitter amplitude accuracy | ± 3 ps ± 10 % typical | | |
| | Adjustable | For each channel independently | | |
| Random jitter (RJ) | Range | 0 to 72 mUI rms (1 UI p-p max.) ¹ | | |
| | Jitter amplitude accuracy | ± 300 fs ± 10 % typical | | |
| | Filters | High-pass: 10 MHz and "off", Low-pass: 100 MHz, Low pass: 500 MHz (for data rates ≥ 3.75 Gb/s), Low pass: 1 GHz (for data rates ≥ 7.5 Gb/s) | Opt. 0G3 | Opt. 0G3 |
| | Adjustable | For each channel independently | | |
| Spectrally distributed RJ according to PCIe 2 (sRJ) ² | Range | 0 to 72 mUI rms (1 UI p-p), ¹ | | |
| | Frequency | LF: 0.01 to 1.5 MHz, HF: 1.5 to 100 MHz | Opt. 0G3 | Opt. 0G3 |
| | Jitter amplitude accuracy | ± 300 fs ± 10 % typical | | |
| | Adjustable | For each channel independently | | |
| Bounded uncorrelated jitter (BUJ) | Range | See HF jitter above ¹ | | |
| | PRBS polynomials | 2 ⁿ -1, n = 7, 8, 9, 10, 11, 15, 23, 31, 33, 39, 41, 45, 49, 51 | | |
| | Filters | 50/100/200 MHz low pass 3rd order | Opt. 0G3 | Opt. 0G3 |
| | Jitter amplitude accuracy | ± 5 ps ± 10% typical for settings shown in table 15 | | |
| | Adjustable | For each channel independently | | |
| | Rate for PRBS generator | 625 Mb/s, 1.25 Gb/s and 2.5 Gb/s | | |
| Clock/2 jitter | Range | ± 20 ps or ± 0.1 UI typical (whatever is less). Note: this means that first eye can be up to 20 ps longer or shorter than subsequent eye. | Opt. 0G3 | Opt. 0G3 |
| | Jitter amplitude accuracy | ± 3 ps typical | | |
| | Adjustable | For each channel independently | | |

1. 1 UI is the maximum sum of RJ, HF-PJ1 and HF-PJ2, spectral RJ, external delay modulation and BUJ.

2. Spectrally distributed random jitter is mutually exclusive with RJ and BUJ.

Table 15. BUJ accuracy applies for these BUJ settings.

| BUJ calibration settings ¹ | Rate for PRBS generator | PRBS polynomial | Low pass filter |
|---------------------------------------|-------------------------|-------------------------|-----------------|
| CEI 6G | 1.25 Gb/s | PRBS 2 ⁹ -1 | 100 MHz |
| CEI 11G | 2.5 Gb/s | PRBS 2 ¹¹ -1 | 200 MHz |
| Gaussian | 2.5 Gb/s | PRBS 2 ³¹ -1 | 100 MHz |

1. Other settings are not calibrated and do not necessarily generate the desired jitter histograms for all data rates of the PRBS generator.

Jitter tolerance specifications (continued)

Table 16. Specifications for Spread Spectrum Clocking (SSC) (requires opt. 0G3: advanced jitter sources).

| | | | M8041A | M8051A |
|-----------------------------|------------------------|--|----------|----------|
| SSC (Spread Spectrum Clock) | Range | 0 to 10,000 ppm (0 to 1%) peak-peak. Select center-spread, up-spread, and down-spread. | | |
| | Frequency | 100 Hz to 200 kHz | | |
| | Modulation | Triangular and arbitrary modulation | Opt. 0G3 | N/A |
| | SSC amplitude accuracy | ± 0.025 % typical | | |
| | Outputs | Can be turned on/off together for CLK OUT, DATA OUT 1, DATA OUT 2, TRG OUT | | |
| Residual SSC (@ PCIe2) | Range | 0 to 100 ps | | |
| | Frequency | 10 to 100 kHz | Opt. 0G3 | Opt. 0G3 |
| | Outputs | Can be turned on/off independently for DATA OUT 1, DATA OUT 2 | | |

Table 17. Specifications for external jitter modulation (DATA MOD IN 1 and 2, CLK MOD IN).

M8041A allows individual jitter injection for data 1, data 2 and clock. M8051A for data 1 and data 2. The option 0G3 is not needed.

| | | | M8041A | M8051A |
|---|-------------|---|--------|--------|
| External jitter - data modulation input 1 and 2 | Description | Input for delay modulation for each DATA OUT individually. | x | |
| | Range | Up to 1 UI ¹ , 0.8 Vpp max | | x |
| | Frequency | Up to 1 GHz | | |
| External jitter - clock modulation input | Description | Input for delay modulation for the TRG OUT and CLK OUT. Affects both. | x | |
| | Range | Up to 1 UI, 0.8 Vpp max | | N/A |
| | Frequency | Up to 1 GHz | | |
| Gain | | 1UI / 0.725 V ± 5% | | |
| Linearity | | 50 mUI | x | x |
| Connectors | | SMA, female | | |

1. 1 UI is the maximum sum of RJ, HF-PJ1 and HF-PJ2, spectral RJ, external delay modulation and BUJ.

Jitter tolerance specifications (continued)

Table 18. Specifications for adjustable Intersymbol Interference (ISI). Adjustable ISI is offered for M8041A and M8051A and requires option 0G5 and serial number >= DE55300500. For lower S/N an upgrade option UG5 is offered, that requires return-to-factory. Adjustable ISI requires M8070A software revision 2.0.0.0 or later.

| | 1 point control (widest range) | 2 point control (best adjust) | M8041A | M8051A | M8061A | M8062A |
|--|--|---|----------|----------|--------|-----------------------|
| Operating range | Emulates loss of real PCB traces for data rates > 5 Gb/s | | | | | |
| Frequency range | 1 to 16 GHz, 1 MHz resolution | | | | | |
| Insertion loss (IL) range for upper point (P1) | No control | -1.5 to -25 dB ¹ | | | | |
| Insertion loss range for lower point (P2) | -0.5 to -25 dB ¹ | -1.5 to -25 dB ¹ | | | | |
| Slope range | -0.5 to -6.0 dB/GHz @ IL offset 0 dB -1.5 to -6 dB/GHz @ IL offset max -2 dB | | | | | |
| Loss resolution | 0.1 dB/GHz typical | | | | | |
| Insertion loss accuracy | ±(0.8 dB + 0.1 dB/GHz) typical | for loss range 0 to -20 dB: ±(0.9 dB + 0.1 dB/GHz) typical | Opt. 0G5 | Opt. 0G5 | No | See M8062A data sheet |
| Presets | M8048A ISI channel 7.7", 9.4", 11.1", 12.8", 14.4", 16.1", 24.4" PCIe3 short and long M-PHY G3A Ch1, G3A Ch2 M-PHY G3B Ch1, G3B Ch2 MIPI-Short, MIPI-Standard, MIPI-Long ² SAS-3 | | | | | |
| Import of S-parameters | Yes, s2p and s4p | | | | | |

1. Within slope range and IL offset range. Frequency of lower point (P2) must be > frequency of upper point (P1).
2. Requires M8070A software revision 2.5.0.0 or later.

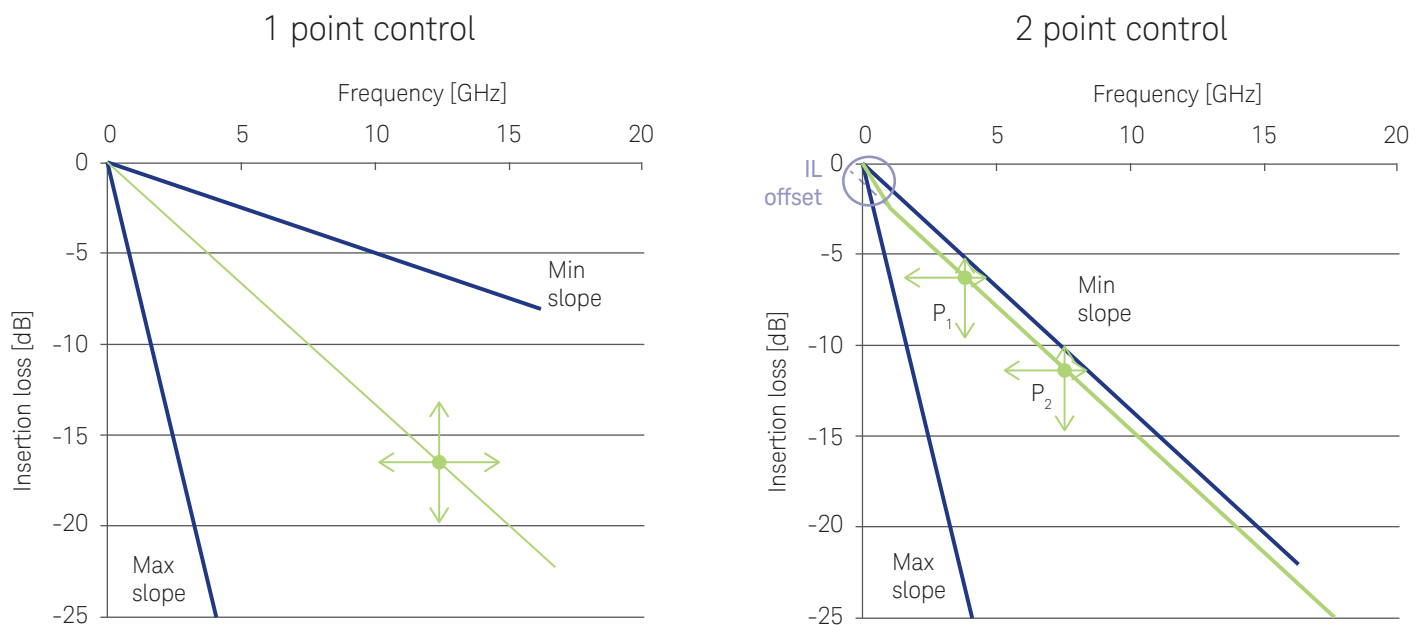


Figure 21. The adjustable ISI can be controlled over a wide range. The chart on the left shows the range for 1 point control. The upper loss point P1 is fix, only the lower point P2 can be varied over a wide range within min and max slope. The chart on the right shows 2 point control which provides full flexibility to adjust the frequency and loss of the upper point 1 and the lower point 2 within the range between min and max slope.

Jitter tolerance specifications (continued)

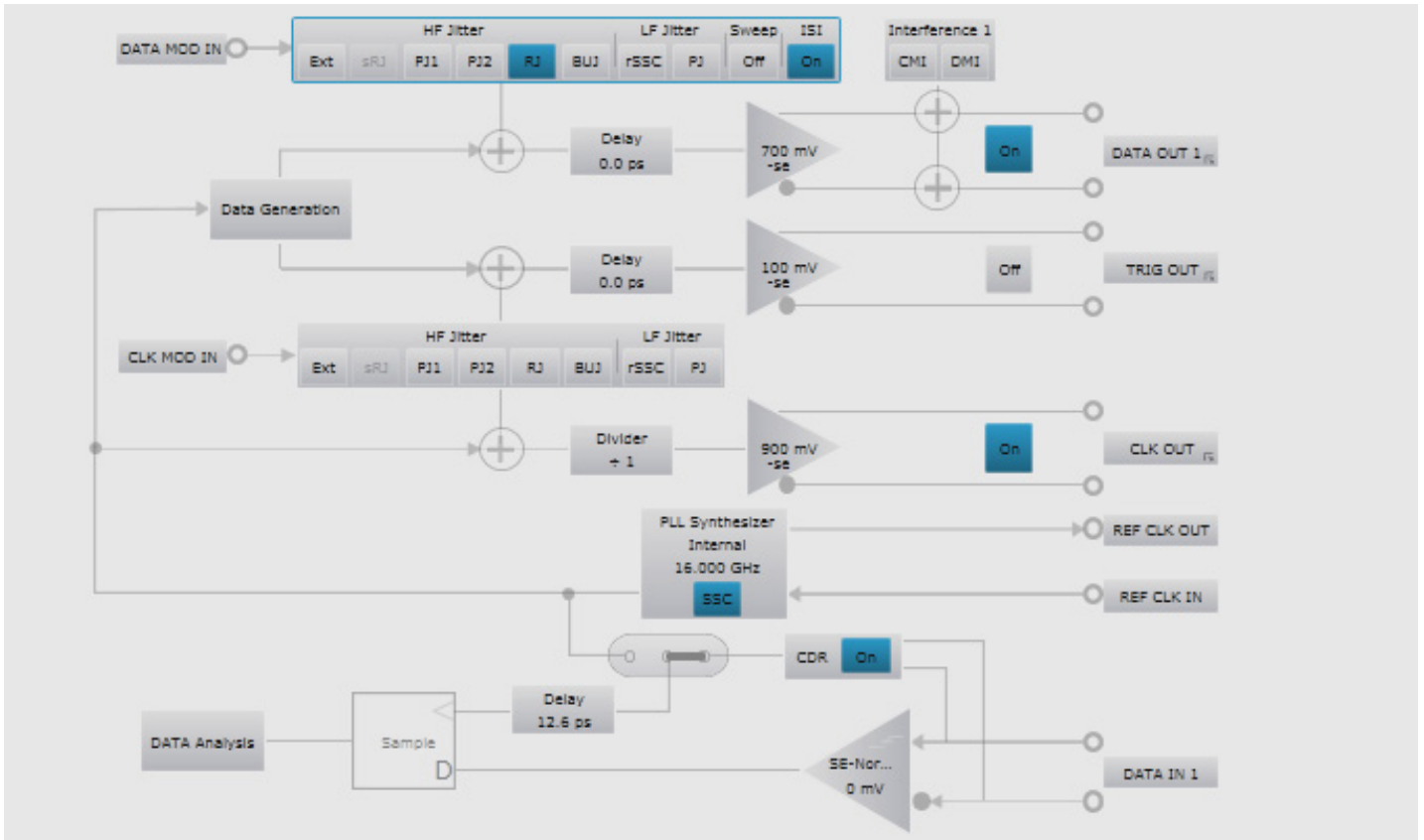


Figure 22. J-BERT M8020A system view for 1 channel.

Jitter tolerance specifications (continued)

ISI channels



External ISI channels are available to emulate channel loss. offers dedicated compliant ISI channels for DisplayPort, PCIe3 (base spec) and SATA. M8048A is offered in addition
For detailed specifications see M8048A data sheet.

M8048A-001 ISI Channels provides four short traces:
7.7”(196 mm), 9.4” (240 mm), 11.12”(282 mm), 12.8”(324 mm)

M8048A-002 ISI Channels provides four long traces:
14.4” (366 mm), 16.1” (408 mm), 24.4” (620 mm), 34.4”(874 mm)

Level interference injection

Common mode and differential mode level interference can be generated internally to test common mode rejection of a receiver and vertical eye closure tolerance. Simultaneous injection of CMI and DMI is possible. In 32 Gb/s configurations with M8061A, external sources for M8061A are required. See M8061A data sheet for details on built-in level interference superposition and gain adjust parameters.

Table 19. Specifications for sinusoidal level interference (CMI, DMI) (requires option 0G7).

| | | | M8041A | M8051A |
|---------------------------------------|--------------------------|--|----------|----------|
| Differential mode interference (DMI) | Amplitude ² | Up to 30% of maximum output amplitude ¹ when "auto range" is enabled. Up to 30% of selected output amplitude range ¹ when "auto range" is disabled. | | |
| | Amplitude accuracy | ±10 mV ±10% typ | | |
| Common mode interference (CMI) | Amplitude ^{2,3} | Up to 320 mV ¹ | Opt. 0G7 | Opt. 0G7 |
| | Amplitude accuracy | ±10 mV ±10% typ | | |
| Modulation frequency | Ranges | LF: 10 MHz to 1 GHz, sinusoidal only HF: 1 GHz to 6 GHz, sinusoidal only | | |
| Simultaneous injection of CMI and DMI | | Yes. HF modulation cannot be used simultaneously for CMI and DMI. LF modulation cannot be used simultaneously for CMI and DMI. See figure below. | | |

1. The maximum output amplitude decreases when CMI or DMI is enabled. See table 2.
2. For each channel independently.
3. Up to 5 GHz.

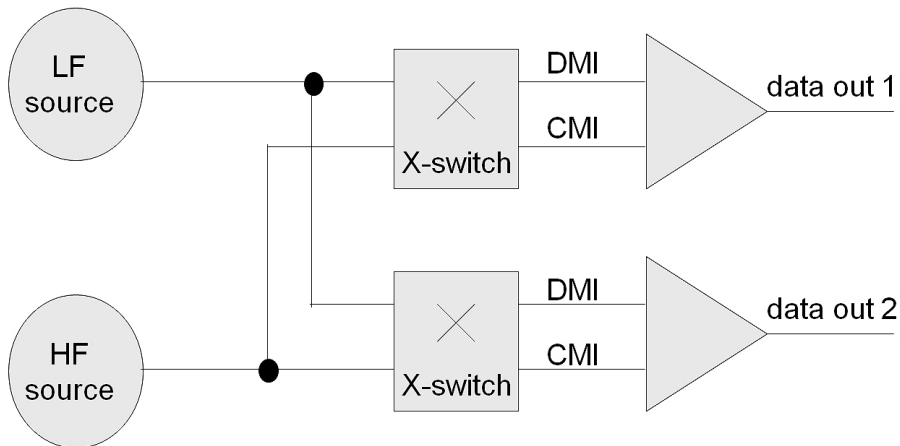


Figure 23. M8020A provides calibrated level interference sources for simultaneous injection of CMI (common mode interference) and DMI (differential mode interference).

Pattern, sequencer and interactive link training

Table 20. Specifications for pattern, sequencer and link training.

| | | M8041A | M8051A | M8061A | M8062A |
|-----------------------------|--|----------|--------|--------|--------|
| PRBS ¹ | 2 ⁿ -1, n = 7, 10, 11, 15, 23, 23p ³ , 31 | | | | |
| PRBS | 2 ⁿ , n = 7, 10, 11, 13, 15, 23 | | | | |
| Mark density | Mark density: PRBS 1/8 to 7/8 | | | | |
| Zero substitution | Yes | x | x | x | x |
| Export/Import | Patterns from N4900 series can be imported | | | | |
| Pattern library | Yes | | | | |
| User definable memory | 2 Gbit/channel ⁴ | | | | |
| Interactive link training | <p>Link training state machine (LTSSM) for PCIe 3⁴ to achieve loopback state via recovery with or without link training. Is suitable for testing downstream and upstream ports according to PCI Express Architecture PHY Test Specification. Supports the following tests:</p> <p>2.3 Add-in Card Transmitter Initial Tx EQ Test for 8 GT/s</p> <p>2.4 Add-in Card Transmitter Link Equalization Response Test for 8 GT/s</p> <p>2.7 System Board Transmitter Link equalization Response Test for 8 GT/s</p> <p>2.10 Add-in Card Receiver Link Equalization Test for 8 GT/s</p> <p>2.11 System Board Receiver Link Equalization Test for 8 GT/s</p> <ul style="list-style-type: none"> - The LTSSM reports to a log file: states, de-emphasis requests by DUT - Supported channels: 1, 2 ² | Opt. 0S1 | N/A | No | No |
| Coding | 8B/10B, 128B/130B, 128B/132B, binary, hex | x | x | No | No |
| Scrambler | PCIe, USB, SATA | x | x | No | No |
| Vector/sequence granularity | 64/80/130/132 bit | x | x | * 2 | * 2 |
| Pattern capture | <p>Yes ⁵</p> <p>Capture on event. Capture n bit before/after event:</p> <ul style="list-style-type: none"> - User defined (minimum) amount of pre-event bits/ symbols and minimum capture bit/symbols - Events: error, CTRL IN A/B, immediate - Max 2 Gbit/ch capture data <p>Save captured data:</p> <ul style="list-style-type: none"> - With errors - As expected data (ignores error content) - As PG data (ignores error content) - Export via pattern editor windows - Export captured data, displays bit & symbol errors - Convert bits into all other codings and vice versa - Ability to mask error bits automatically <p>Display of captured data:</p> <ul style="list-style-type: none"> - Display errors with color coding - Navigate through error bits/symbols (find next/previous) | x | x | N/A | No |
| Pattern sequencer | 3 counted loop levels, 1 infinite loop, # of blocks: 500 | x | x | x | x |

1. Note: polarity is inverted compared to ParBERT and J-BERT N4903A/B and N49xx models.

2. For availability: contact factory. Free software update.

3. Modified compliance pattern for PCIe3.

4. Requires M8070A software revision 1.5.0.0 or later. Free upgrade (interactive link training requires option 0S1).

5. Requires M8070A software revision 2.0.0.0 or later.

Pattern, sequencer and interactive link training (continued)

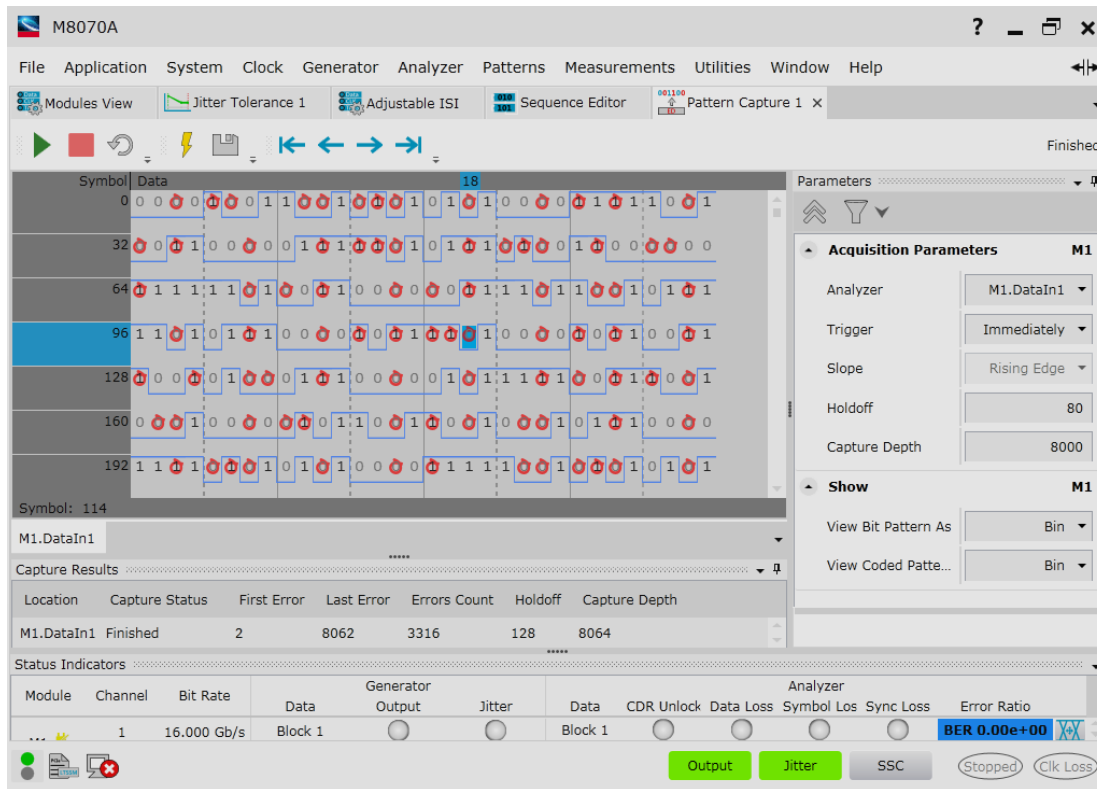


Figure 24. The J-BERT M8020A analyzer can capture up to 2 Gbit per channel. Capture events and depth can be defined. The captured pattern can be exported and loaded as generator pattern or as expected pattern for further error analysis. The example shows errored bits in red with navigation arrows.

Specifications analyzer (error detector)

Each M8041A/51A analyzer channel includes a clock recovery.

For the following functions a separate module option is required:

- Equalizer CTLE option (option 0A3 for M8041A and M8051A)
- SER/FER analysis (option 0S2 is offered for M8041A only, but applies for all analyzers channels in the same clock group): this option provides handling of 8B/10B coded, 128B/130B coded and 128B/132B coded patterns. 8B/10B coded patterns support automatic handling of running disparity changes, scrambling/descrambling and up to 4 filler primitives consisting of up to 4 symbols each. No dead time while filtering filler symbols. Supports changes of length of 128B/130B and 128B/132B coded Skip Ordered Sets for PCIe und USB 3.1.
- For 32 Gb/s setups the N4877A-232 CDR and Demultiplexer is required to use the M8020A analysis functions. Please refer to the N4877A data sheet for details on the 32Gb/s input specifications. All parameters of the N4877A can be controlled via the M8070A system software when the "mux and demux" configuration is selected (requires M8070A software revision 1.5.0.0.or later). The CTLE and SER/FER analysis are not available for 32 Gb/s configurations with M8061A and N4877A.

Table 21. Specifications for analyzer / error detector (Option C08 or C16).

| | | M8041A | M8051A |
|--------------------------------|--|----------|----------|
| Data rate | 256 Mb/s to 8.50 Gb/s (opt. C08), 256 Mb/s to 16.20 Gb/s (opt. C16) | | |
| Channels per module | 1 or 2 (opt. 0A2) | | |
| Data format | NRZ, single ended and differential | | |
| Input sensitivity ¹ | 50 mV typical @ normal sensitivity mode ⁴ 40 mV typical @ high sensitivity mode ⁴ | | |
| Input voltage window | -1.0 V to + 3.3 V | X | X |
| Maximum voltage window | 1.0 Vpp single ended @ normal sensitivity mode 0.50 Vpp single ended @ high-sensitivity mode | | |
| Termination voltage | -1.0 V to + 3.3 V ³ | | |
| Timing resolution | 1 mUI | | |
| Input bandwidth | 17.5 GHz typical | | |
| CTLE | Yes. The following presets are available: PCIe 3.0 @ 8 Gb/s: -6.0 dB, -9 dB, -12 dB PCIe 4.0 @16 Gb/s: ⁵ -6 dB, -9 dB, -12 dB USB 3.0 @ 5 Gb/s USB 3.1 @ 10 Gb/s: ⁵ 0 dB, -3 dB, -6 dB | Opt. 0A3 | Opt. 0A3 |
| Clock data recovery | Yes for each input channel. See table 21 for more details. | | |
| Sampling point | Manual and automatic. Finds optimum voltage threshold and delay of the sampling point. Delay accuracy ± 30 mUI | | |
| Decision threshold range | -1.0 V to + 3.3 V in 1 mV steps. Must be within ± 0.5 V range from common mode voltage. Threshold accuracy ± 25 mV | X | X |
| Phase margin | 1 UI - 16 ps typical for PRBS 2 ¹⁵ - 1 1 UI - 7 ps typical for clock pattern | | |
| Interface | Differential: 100 Ω , single ended: 50 Ω , DC coupled | X | X |
| Data input connectors | 3.5 mm, female | | |

1. Measured with PRBS 2³¹ - 1 at 16 Gb/s, AC coupling mode, BER of 10⁻¹², CTLE disabled.

2. For availability please contact factory.

3. Termination voltage must be within a window of DC common mode voltage ± 1.7 V.

4. Eye height measured at input of reference cable M8041A-801 with DCA-X module 86117A. Applies for single ended and differential input signals.

5. Requires M8070A software revision 2.5.0.0. or later and a S/N of \geq DE55300700 or \geq MY55300800

Specifications analyzer (error detector) (continued)

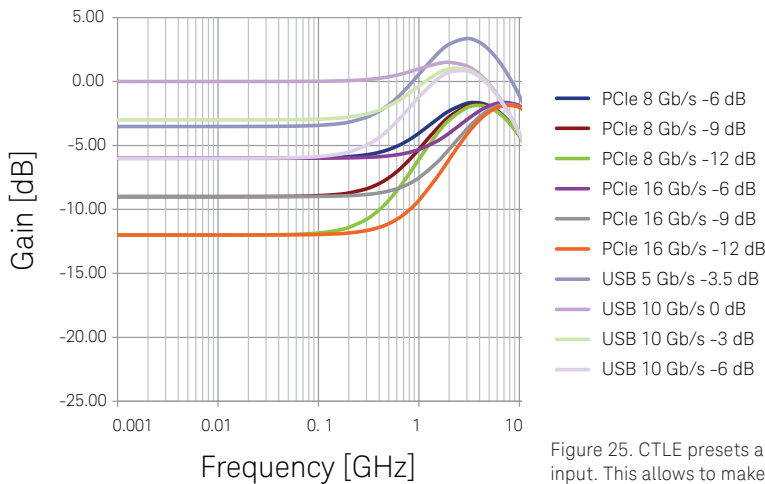


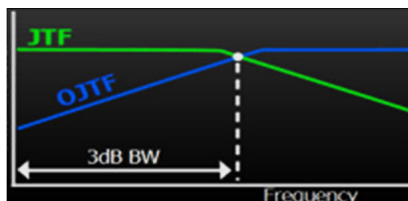
Figure 25. CTLE presets are available for each M8041A/51A analyzer input. This allows to make BER measurements even on closed eyes.

Table 22. Specifications for clock recovery.

| | Condition | M8041A | M8051A |
|--|---|--|--------|
| CDR data rate range | 1.0125 to 16.2 Gb/s | | |
| Selectable loop type | 1st and 2nd order PLL - see figure below for description | | |
| Tunable loop bandwidth | 102 kHz to 20 MHz depends on data rate as shown in figure below. | | |
| | Data rate/ 10000 to data rate/ 500 ^{2,3} | Data rate from 1.0125 Gb/s to < 8.1 Gb/s, transition density of 50 % | |
| | Data rate/ 10000 to data rate/ 660 ^{2,3} | Data rate > 8.1 Gb/s, transition density of 50% | |
| Loop bandwidth accuracy | ± 20% typical | 1 MHz < loop BW < data rate/ 900, transition density of 50% and peaking ≤ 2 dB | |
| Tunable peaking range | 0.. 3 dB @loop BW ≤ data rate/ 900 0.. 1 dB @loop BW > data rate/ 900 | With type 2 second order loop selected | x x |
| Transition density compensation | The user can set the expected transition density and the loop compensates the loop bandwidth accordingly | | |
| Tracking range (maximum frequency deviation) | Frequency deviation [ppm]= ±(9000 - 350*data rate[Gb/s]) | With type 2 selected and loop BW ≥ data rate / 800, Software revision 3.0.0.0 and higher ¹⁾ | |
| CDR freeze | After 256 consecutive bits without transition the CDR goes automatically into a freeze state. At every transition the CDR recovers from the freeze state. | If CDR is enabled | |

First order PLL (type 1)

- A type 1 is defined by bandwidth. No peaking.
- JTF bandwidth = OJTF bandwidth.
- Used by some communication standards



Second order PLL (type 2)

- This type 2 is defined by JTF loop bandwidth and peaking.
- JTF bandwidth > OJTF bandwidth.
- Used by some computing standards.

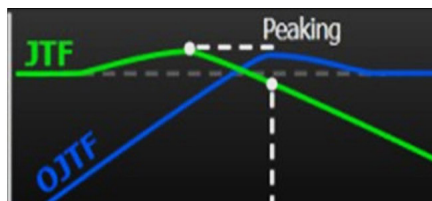


Figure 26. Each M8041A/51A analyzer has a built-in clock recovery. Choose between first and second order PLL.

1. Tracking range for older software versions: Frequency deviation [ppm]= ±(9000 - 500*data rate[Gb/s])

Specifications analyzer (error detector) (continued)

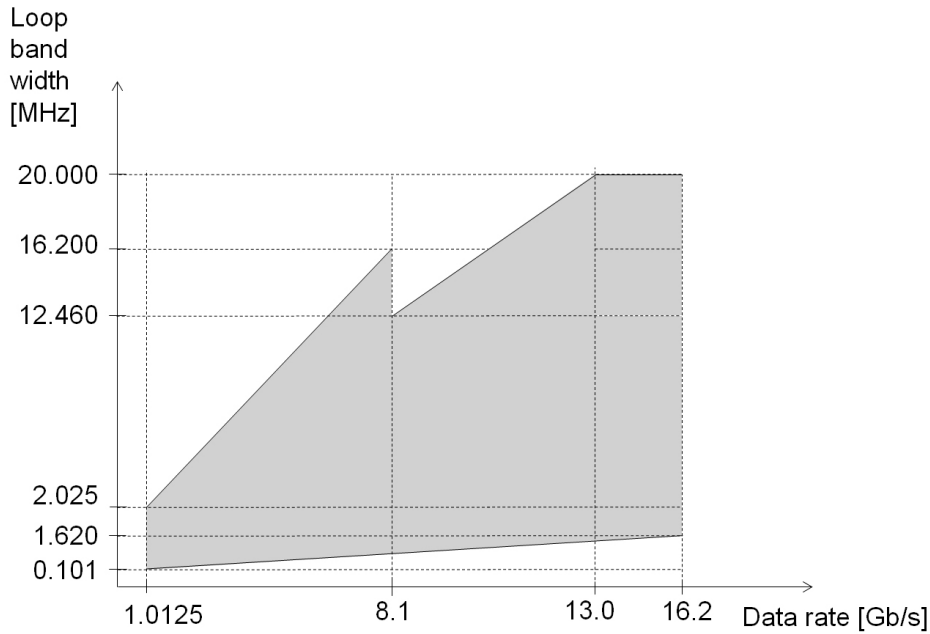


Figure 27. CDR loop bandwidth range for a transition density of 50%

Table 23. Measurement capabilities (Option C08 or C16).

| | | M8041A | M8051A | M8061A | M8062A |
|----------------------------------|---|----------|--------|--------|--------|
| BER | Accumulation and instant | x | x | x | x |
| BERT Scan with RJ, DJ separation | Yes, up to 16.2 Gb/s and PRBS $2^{31} - 1$ | x | x | No | x |
| Jitter tolerance | Yes | x | x | x | x |
| Eye contour | Yes ¹ | x | x | No | x |
| Quick eye diagram | Yes ¹ | x | x | No | No |
| Output level and Q factor | Yes ³ | x | x | No | No |
| Bit recovery mode | Yes ¹ | x | x | N/A | No |
| Symbol/Frame error rate | 8B/10B, 128B/130B, 128B/132B ² coded and retimed patterns | | | | |
| Filtering of filler symbols | Automatic removal of filler symbols. See also the description above. | | | | |
| Counters | 8B/10B: compared symbols, errored symbols, illegal symbols, filler symbols, wrong disparity, frames, errored frames 128B/130B: blocks, errored blocks, illegal sync headers, filler symbols, modified filler symbols 128B/132B ² : blocks, errored blocks, illegal sync headers, filler symbols, modified filler symbols, corrected sync headers | Opt. OS2 | N/A | No | No |

1. Requires software 3.0.0.0 or higher. Free software update.

2. 128B/132B SER/FER, filler symbol removal and counters are supported for data rates from 9 to 11 Gb/s (USB 3.1). Requires software revision 1.5.0.0 or later.

3. Requires software revision 2.0.0.0 or later.

User interface and remote control

The M8070A system software for the M8000 Series of BER Test Solutions is required to control M8041A, M8051A, M8061A, and M8062A.

Table 24. User interface and remote control interface.

| System software | M8070A |
|---|--|
| Software licensing | Offline version does not require a license. For controlling the hardware you can choose between a transportable, perpetual license (M8070A-OTP) and a network, perpetual license (M8070A-ONP) . The network license is only recommended when using multiple M8020A setups within one company. When ordering M8020A-BU1 the M8070A-OTP license will be pre-installed on the embedded controller. |
| Controller requirements | Embedded PC: Choose M8020A-BU1 for a pre-installed embedded controller M9536A including pre-installation of M8070A software and module licenses. Otherwise: M9536A 1-slot AXLe embedded controller, choose options for Windows 7 or 8, 8 or 16 GB RAM, USB External PC: USB connection recommended between external PC and AXLe chassis. Minimum of 8 GB RAM recommended. For PCIe connectivity please refer to list of tested PCs for AXLe Technical Note, pub no. 5990-7632EN |
| Operating system | Microsoft Windows 7 (64 bit) SP1, Windows 8 (64 bit), Windows 8.1 (64 bit) |
| Controller connectivity with AXLe chassis | USB 2.0 (Mini-B) recommended, PCIe 2.0/8x (only for highest data throughput and desktop PC) |
| Programming language | SCPI. Not compatible with N4900 series and ParBERT 81250A |
| Remote control interface | Desktop or Laptop PC: LAN M9536A: LAN |
| Save/Recall | Yes |
| Export of measurement results | Jitter tolerance results as *.csv file |
| Display resolution | Minimum requirement 1024 x 768 |
| Scripting interface | The built-in scripting engine is based on IronPython. It enables the control of the device under test as well as other test equipment. Function hooks are available to tailor your measurements, such as read-out of built-in error counters or initializing the device. |
| DUT control interface | Enables access to built-in error counters and status registers of a device under test (BIST) for use with automated measurements like accumulated BER and jitter tolerance. Can also be used to customize the measurements to DUT specific needs. IronPython scripting and .net libraries are supported to interface with the DUT. Requires option M8070A-1TP or -1NP |
| Command expert | Yes |
| Software pre-requisites | Microsoft Win 7 SP1 or 8 / 8.1, IO library rev. 16.3 |

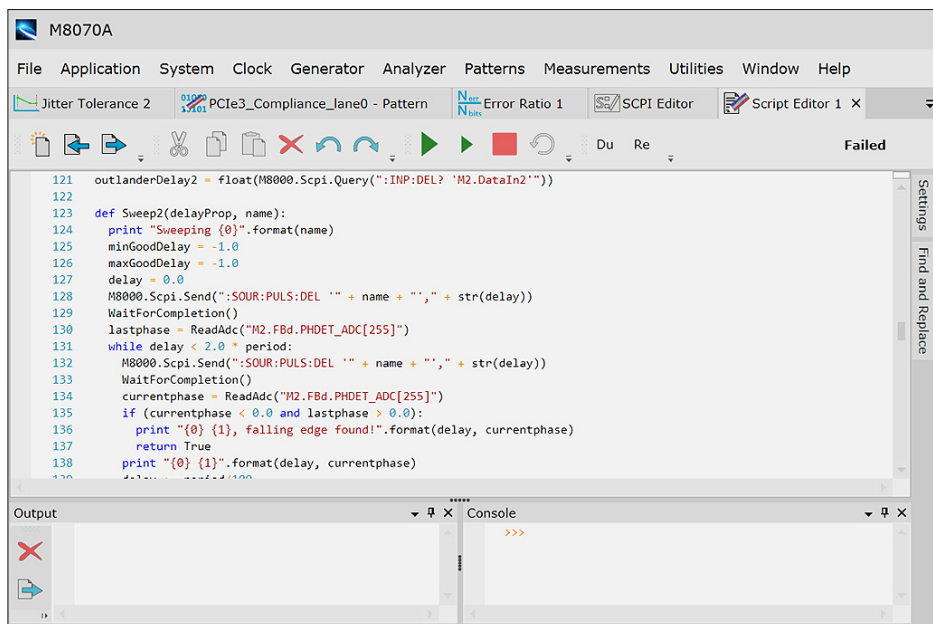


Figure 28. The built-in scripting engine of J-BERT M8020A allows to communicate with the DUT or other instruments. The scripting language is Iron Python.

General characteristics and physical dimensions

Table 25. General characteristics for M8041A and M8051A modules.

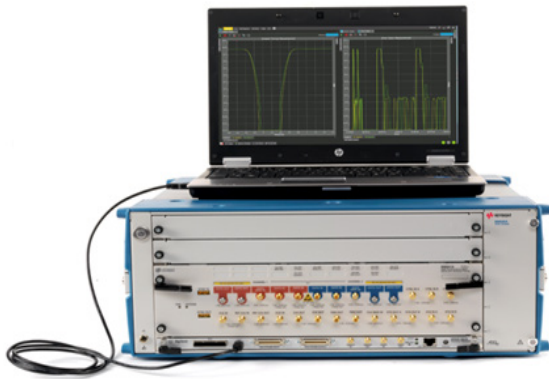
| | M8041A | M8051A |
|---|---|--|
| Operating temperature | 5 °C to 40 °C (41 °F to + 104 °F) | |
| Storage temperature | -40 °C to +70 °C (modules) (-40 °F to + 158 °F) | |
| Operating humidity | 15% to 95% relative humidity at 40°C (non-condensing) | |
| Storage humidity | 24% to 90% relative humidity at 65°C (non-condensing) | |
| Power requirements (module only) | 350 W | 250 W |
| Physical dimensions for modules (W x H x D) | 3- slot AXle module: 351 x 92 x 315 mm (13.8 x 3.6 x 12.4 inch) | 2-slot AXle module: 351 x 61 x 315 mm (13.8 x 2.4 x 12.4 inch) |
| Physical dimensions for M8020A-BU1/-BU2 (W x H x D) | Installed in 5-slot AXle chassis: 463 x 194 x 446 mm (18.2 x 7.6 x 17.6 inch) | |
| Weight net | M8041A module: 6.6 kg (14.6 lb) With M8020A-BU1: 24 kg (53 lb) With M8020A-BU2: 19.9 kg (43.9 lb) | M8051A module: 5.0 kg (11.0 lb) In bundle with M8041A and in a 5-slot chassis: 24.9 kg (54.9 lb) |
| Weight shipping | With M8020A-BU1: 37 kg (82 lb) With M8020A-BU2: 32.5 kg (71.7 lb) | N/A |
| Recommended recalibration period | 1 year | |
| Warranty period | 3 years return to | |
| Warm-up time | 30 minutes | |
| Cooling requirements | Slot airflow direction is from right to left. When operating the M8041A/51A choose a location that provides at least 50 mm of clearance at each side. See also start-up guide for M9505A chassis. | |
| EMC | IEC 61326-1 | |
| Safety | IEC 61010-1 | |
| Quality management | ISO 9001, 14001 | |

Specification assumptions

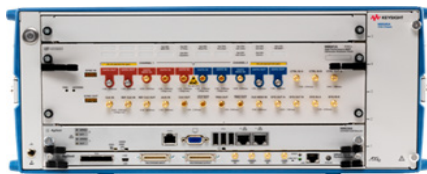
The specifications in this document describe the instruments' warranted performance. Preliminary values are written in *italic*. Non-warranted values are described as typical. All specifications are valid in the specified operating temperature range after the warm-up time and after auto-adjustment. If not otherwise stated all outputs need to be terminated with 50 Ω to GND. All M8041A and M8051A specifications if not otherwise stated are valid for transition times set to “steep”, and using the recommended cable pair M8041A-801 (2.92 mm, 0.85 m, matched pair).

Ordering instructions

Please refer to the *J-BERT M8020A High-Performance BERT - Configuration Guide (5991-4032EN)* for ordering details.



M8020A-BU2
16 Gb/s High-performance BERT, 1-2 channel
with external PC



M8020A-BU1
with embedded PC



16 Gb/s High-performance BERT, 3-4 channel
(external PC not shown)



32 Gb/s High-performance BERT, 1 channel with M8061A/62A
(external PC not shown). Setup with M8061A requires N4877A as CDR/Demux.

Figure 29. Overview of possible J-BERT M8020A configurations.

Default accessories included with shipment:

M8041A module: eight 50 Ω terminations, commercial calibration report (“UK6”), certificate of calibration, ESD protection kit.

M8051A module: four 50 Ω terminations, clock synchronization cable (M8051A-801), commercial calibration report (“UK6”), certificate of calibration

M8061A module: see M8061A data sheet

M8062A module: see M8062A data sheet

M8020A-BU1: M9505A AXIe chassis with embedded controller, USB cable, getting started guide, AXIe filler panel, power cord

M8020A-BU2: M9505A AXIe chassis, USB cable, getting started guide, AXIe filler panel, power cord

M8070A: CD-ROM with M8070A system software

Recommended accessories:

| | |
|---|------------|
| Matched cable pair, 2.92 mm (m) to 2.92 mm (m), 0.85 m (Recommended for each data output of M8041A/51A. This 2.92 mm cable is compatible with 3.5 mm front panel connectors of M8041A/51A.) | M8041A-801 |
| Bandpass filter 11.4 to 15.6 GHz, SMA (For use with M8061A in clock path to minimize intrinsic RJ of M8061A for data rate of 25.78 Gb/s.) | M8061A-802 |
| Bandpass filter 11.1 to 17.5 GHz, SMA (For use with M8061A in clock path to minimize intrinsic RJ of M8061A for data rates from 25.0 to 32.0 Gb/s) | M8061A-803 |
| Cable kit for connecting M8061A with M8020A, 3x 3.5 mm, 0.6 m | M8061A-804 |
| DC block, 26 GHz, 3.5 mm | N9398C |
| ISI channels, four short traces | M8048A-001 |
| ISI channels, four long traces | M8048A-002 |
| Short matched cable pair, SMA (m) to SMA (m) for cascading M8048A ISI channels | M8048A-801 |
| Four SMA cables, unmatched | 15442A |
| Rack-mount kit for AXIe 5-slot chassis M9505A | Y1226A |

Test automation software with support of M8020A

| | |
|---|------------|
| Test automation software for PCIe receiver test | N5990A-101 |
| Test automation software for USB receiver test | N5990A-102 |
| Test automation software for SATA receiver test | N5990A-103 |
| Test automation software for DisplayPort | N5590A-155 |
| Test automation software for MIPI M-PHY | N5590A-165 |
| USB link training suite | N5990A-302 |
| SATA link training suite | N5990A-303 |
| MIPI M-PHY frame generator | N5590A-365 |
| PCIe link training suite | N5990A-301 |
| PCIe link equalization tests | N5990A-501 |
| Test automation software, core | N5990A-010 |

Warranty, calibration and productivity services:

| | |
|--------------------------------------|----------------------|
| Extended 5 year warranty Return-to- | R1280 (R-51B-001-5Z) |
| Calibration services (3 and 5 years) | R1282 |
| Productivity assistance | R1380-M8000 |

Related literature

Data sheets and configuration guides:

| | |
|--|-------------|
| <i>M8048A ISI Channels, Data Sheet</i> | 5991-3548EN |
| <i>M8061A Multiplexer with De-Emphasis, Data Sheet</i> | 5991-2506EN |
| <i>M8062A 32Gb/s BERT Front-End, Data Sheet</i> | 5992-0987EN |
| <i>M8030A Multi-channel BERT, Data Sheet</i> | 5992-1287EN |
| <i>J-BERT N4903B high-performance BERT, Data Sheet</i> | 5990-3217EN |
| <i>N4877A and N1075A CDR/Demux, Data Sheet</i> | 5990-9949EN |
| <i>M9505A AXIe Chassis 5-slot, Data Sheet</i> | 5990-6584EN |
| <i>J-BERT M8020A, Configuration Guide</i> | 5991-4032EN |

Application notes:

| | |
|---|-------------|
| <i>Master your MIPI M-PHY receiver test using J-BERT M8020A, Application Brief</i> | 5991-3959EN |
| <i>How to pass receiver test according PCI Express CEM specification, Application Note</i> | 5990-9208EN |
| <i>Accurate calibration of PCIe 3.0 receiver stress signals, Application Note</i> | 5990-6599EN |
| <i>How to test a MIPI M-PHY high-speed receiver, Application Note</i> | 5991-2848EN |
| <i>Master your next PCIe3 receiver test using J-BERT M8020A, Application Note</i> | 5991-4190EN |
| <i>Master your next USB 3.x designs with J-BERT M8020A, Application Note</i> | 5991-4357EN |
| <i>Characterizing and verifying compliance of 100Gb Ethernet components and systems, Application Note</i> | 5992-0019EN |

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